Using HARDSIL® to minimize the impact of extreme temperature on CMOS integrated circuits

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Introduction

There is a growing trend to increase the sophistication of electronics in high temperature systems with more advanced CMOS devices that can be operated at high temperatures. This is being driven by the desire to enhance electronic controller systems for extreme environment applications such as avionics, downhole drilling, alternative energy and now expanding to the Internet of things.

A major challenge facing designers of such systems is that many of the commercial IC components used to build such systems are not rated for operation at high temperature and *their reliability is at risk when used at temperatures > 125˚C.*

Commercially available digital and analog CMOS devices mainly operate in moderate temperature environments but designers want electronic systems intended for use in extreme temperature environments to deliver the same high level of functionality, integration and reliability as commercial devices while operating at temperatures of up to 200˚C.

Unfortunately, due to the limited number of high temperature rated CMOS products that are available, system developers are often forced to choose a commercial off-the shelf (COTS) device was not designed for operation at temperatures greater than 125˚C.

A CMOS device operating at a temperature greater than 125˚C is likely to experience significantly higher rates of failures than it would when operating at temperatures < 125˚C. System developers must therefore take precautions at the architectural level to protect the system from high temperature effects. This is often accomplished by building in heat dissipation methodologies which add cost, size, weight and power (SWAP). Ideally, a designer could simply select an appropriate CMOS device that could withstand *high temperatures* up to 200˚C.

CMOS Latch-up

All bulk CMOS devices are subject to latch-up. Latch-up effects range from transient failures that upset the logic state of the circuit, functionally disabling regions of the circuit or destroying the device (hard failure).

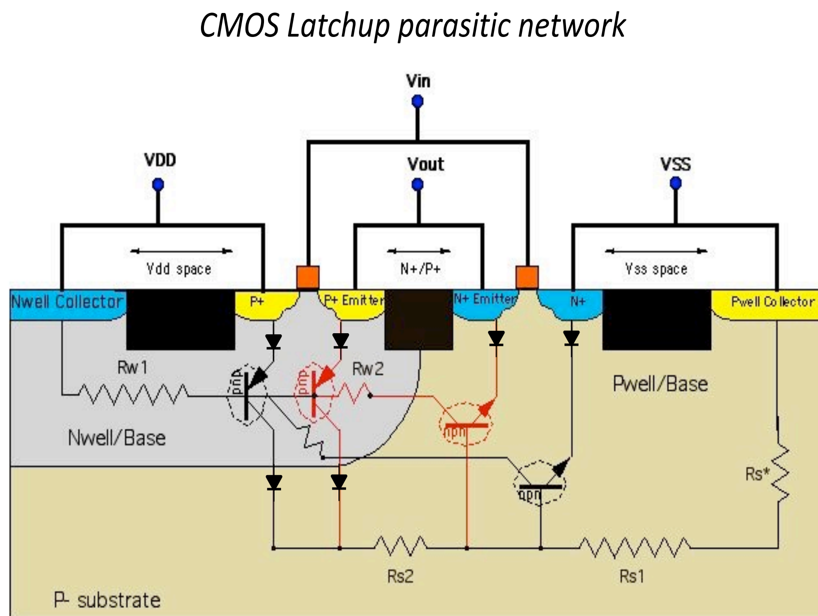
Latch-up occurs due to parasitic devices that are created across a bulk CMOS wafer that become problematic when there is a transient event that has the effect of switching on the parasitic structure. The parasitic transistors are configured in such a way that any current flowing through one device is amplified by the other BJT and this positive feedback loop results in a short circuit from VDD to VSS. The parasitic structure resembles a silicon controlled rectifier (SCR) and is shown in Figure 1.

Increasing temperature reduces the forward bias voltage of the p-n diode, making it easier for a transient event (neutron, single over-voltage, current noise, or single particle) to trigger the parasitic bi-polar transistor structure into an “on” state. The reduction of the diode forward bias caused by the increasing temperature reduces latch-up trigger current as the diode is more easily forward biased and this leads to increased possibility of failure.

As temperature is increased, the device becomes more susceptible to latch-up because the effectiveness of a p-n diode to block current is degraded with temperature. Increasing temperature results in increased p-n junction diode leakage current as electron-hole pairs are generated in the silicon lattice of the semiconductor

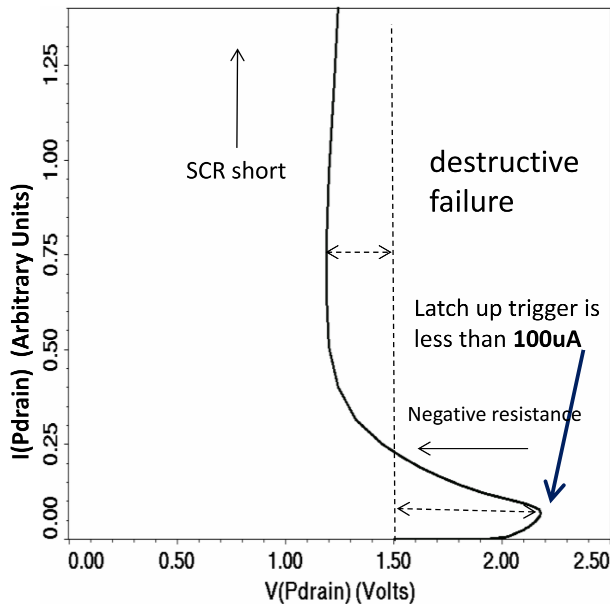
device and collected at the cathode/anode terminals. The p-n junction diode forward-biasing shifts to depletion, making the diode easier to turn on. This leads to increased transient failures ranging from micro-latch triggering, destructive latch-up or simple forward diode conduction (high leakage). Micro-latch triggering is a subset of the latch-up phenomenon where the device current remains below the maximum specified for the device and is difficult to observe directly within the CMOS circuit core regions. It is instead observed as high leakage current.

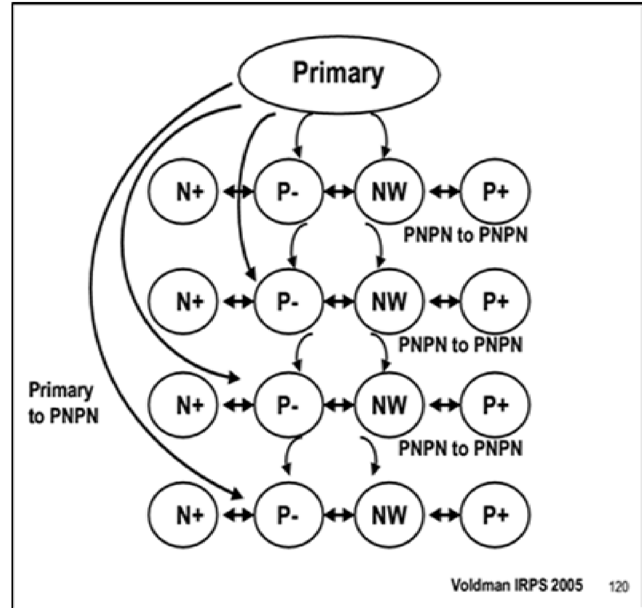
Figure 1 - CMOS twin well cross section with the electrical schematic of the parasitic network of diodes and BJTs.



Although micro latch-up may not result in the destruction of a chip (but it will certainly result in increased power consumption and self-heating), if parasitic charge spreading occurs, chip destruction becomes more likely. Parasitic charge spreading of a latch-up event across CMOS diffusions will extend the latch-up transient from the initial parasitic diffusion to couple (via parasitic bipolar interactions) with other regions of the circuit that were initially unaffected. As CMOS processes scale to smaller geometries, transistor and isolation well diffusions are in closer proximity to each other. This proximity makes it easier for parasitic transient interactions to occur. These events can trigger active conduction by a transient event such as over-voltage, ESD spike, ionizing particle strike or high temperature leakage. Figure 2 illustrates an over-voltage event initiating latch-up and the effect of parasitic interactions between different circuit localities.

Figure 2 - (Left) IV plot of a latch-up over-voltage transient showing the rise of the signal over-voltage initiating latch-up triggering, negative resistance region and latch-up saturation (SCR short). (Right) Voldman (IRPS 2005) illustrates the CMOS parasitic interactions.



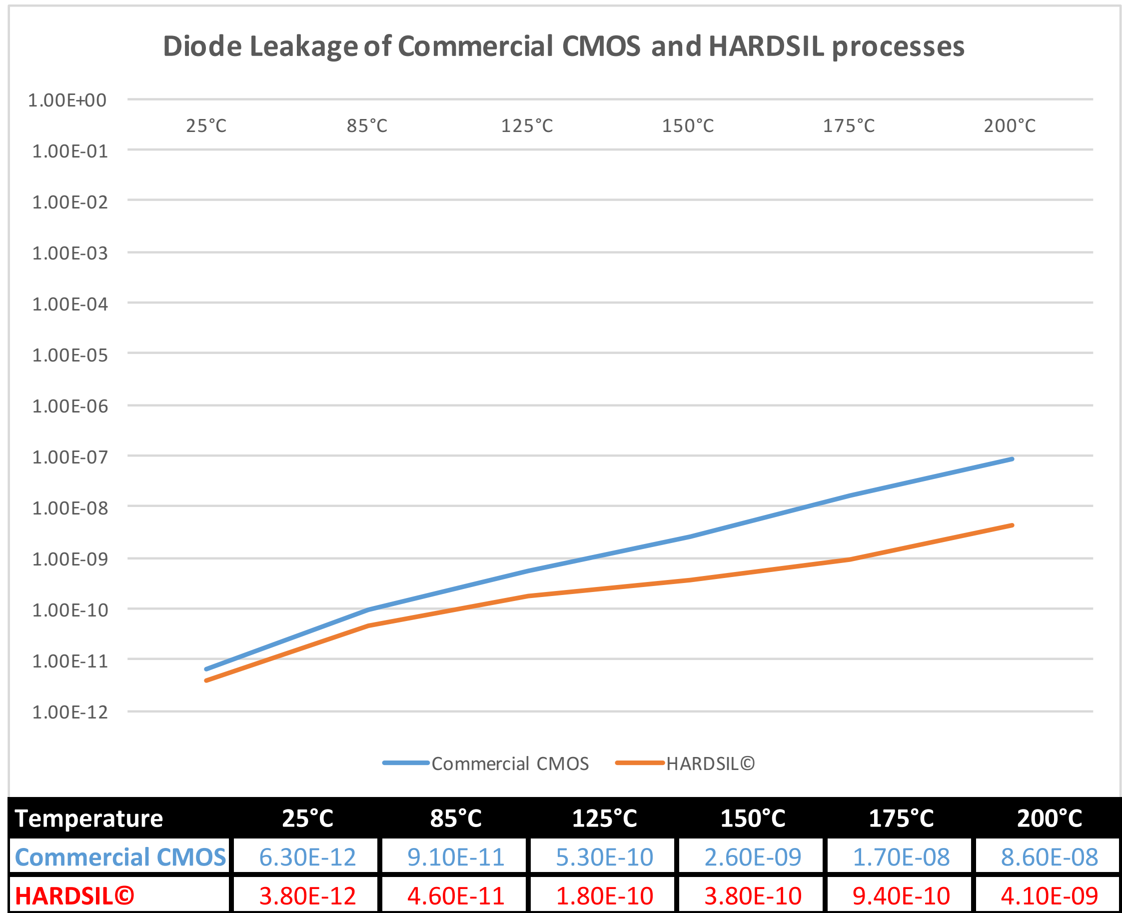


Introduction to HARDSIL© and Buried Guard Ring (BGR) Technology

HARDSIL© is VORAGO Technologies patented process to harden CMOS devices against the effects of extreme temperature and radiation. Any commercial CMOS manufacturing process that has been enhanced with HARDSIL© will be latch-up immune to all forms of natural radiation and extreme temperatures up to 200˚C.

A Buried Guard Ring (BGR) is created in the CMOS structure as part of the HARDSIL© process. When implemented into the process, the BGR enables any CMOS circuit to operate latch-up free at temperatures > 200˚C. The BGR reduces diode current leakage at high temperature by reducing minority carrier lifetimes and significantly improving the grounding plane across the CMOS device structure with a low resistance shunt within the P-type silicon. This shunt pins the Pwell potential to 0 V and hardens the parasitic N+/P- emitter, preventing forward bias. To demonstrate the effect of HARDSIL© on diode leakage, two identical test structures were developed and observed over temperature. The results indicated that the diode leakage current was significantly less temperature dependent than the commercial CMOS device. A graph showing these results is given in Figure 3 (the current leakage on the Y-axis has a log scale). The HARDSIL© treated structure exhibits more than twenty times less leakage than the commercial CMOS structure.

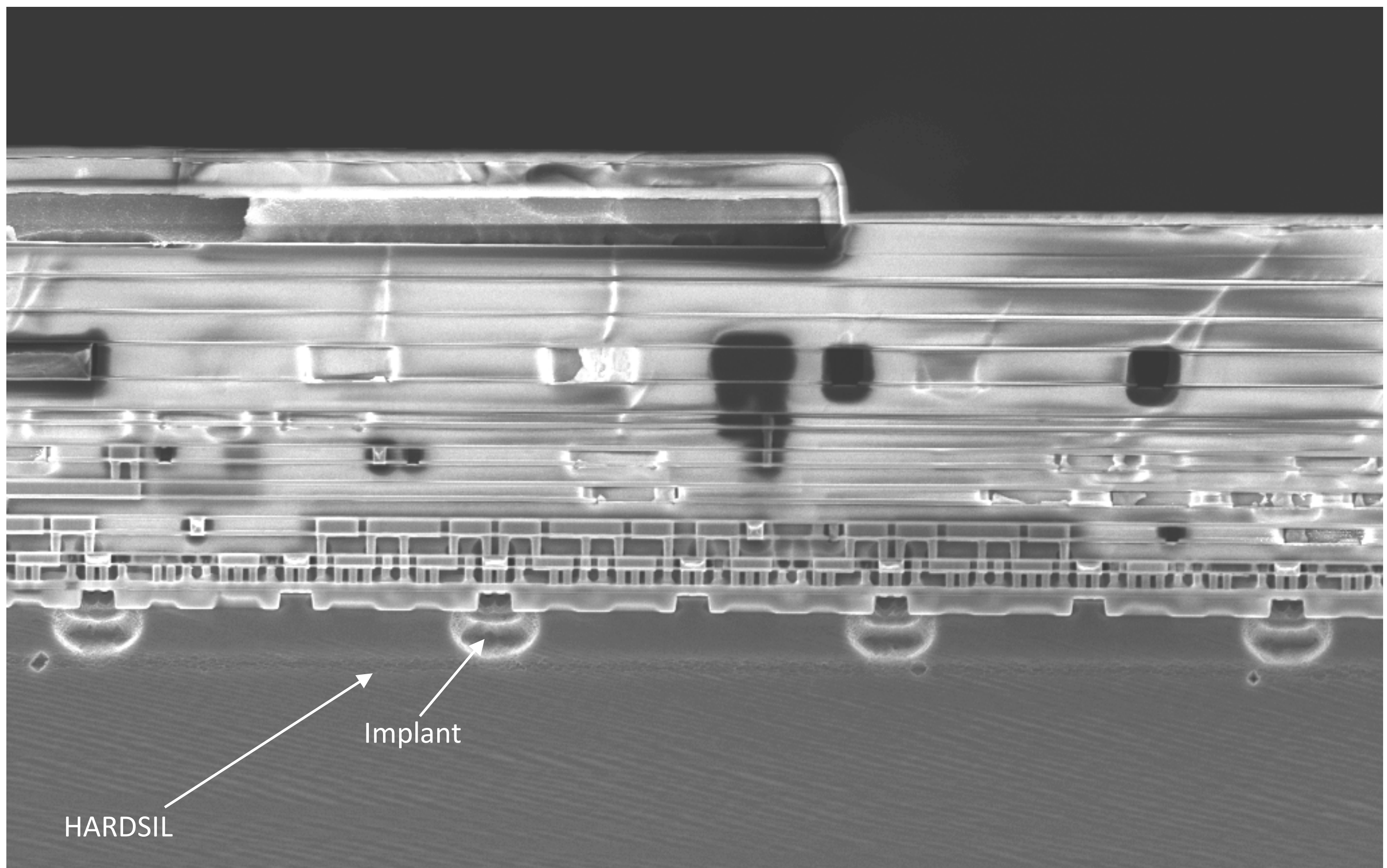
Figure 3 - HARDSIL© process diode leakage is considerably less at elevated temperatures than commercial CMOS



Temperature	25°C	85°C	125°C	150°C	175°C	200°C
Commercial CMOS	6.30E-12	9.10E-11	5.30E-10	2.60E-09	1.70E-08	8.60E-08
HARDSIL©	3.80E-12	4.60E-11	1.80E-10	3.80E-10	9.40E-10	4.10E-09

The BGR implemented on a VORAGO Technologies VA10800 microcontroller is shown in Figure 4. The area above the light horizontal line is a highly conductive layer beneath the CMOS structures that reduces substrate resistance and prevents the parasitic BJTs from switching on. This is the mechanism that prevents latch-up from occurring. There is also a vertical implant that provides a highly conductive connection to the well contacts.

Figure 4 – HARDSIL© BGR on VORAGO Technologies VA10800 microcontroller



A CMOS circuit with BGR implemented cannot be triggered into latch-up by any on-chip parasitic SCR structure. The BGR structure eliminates latch-up by establishing a low resistance shunt throughout the chip which prevents diode forward biasing which acts to limit the activation of the parasitic n-emitters.

Latch-up Testing Comparison Between HARDSIL© and Commercial Devices

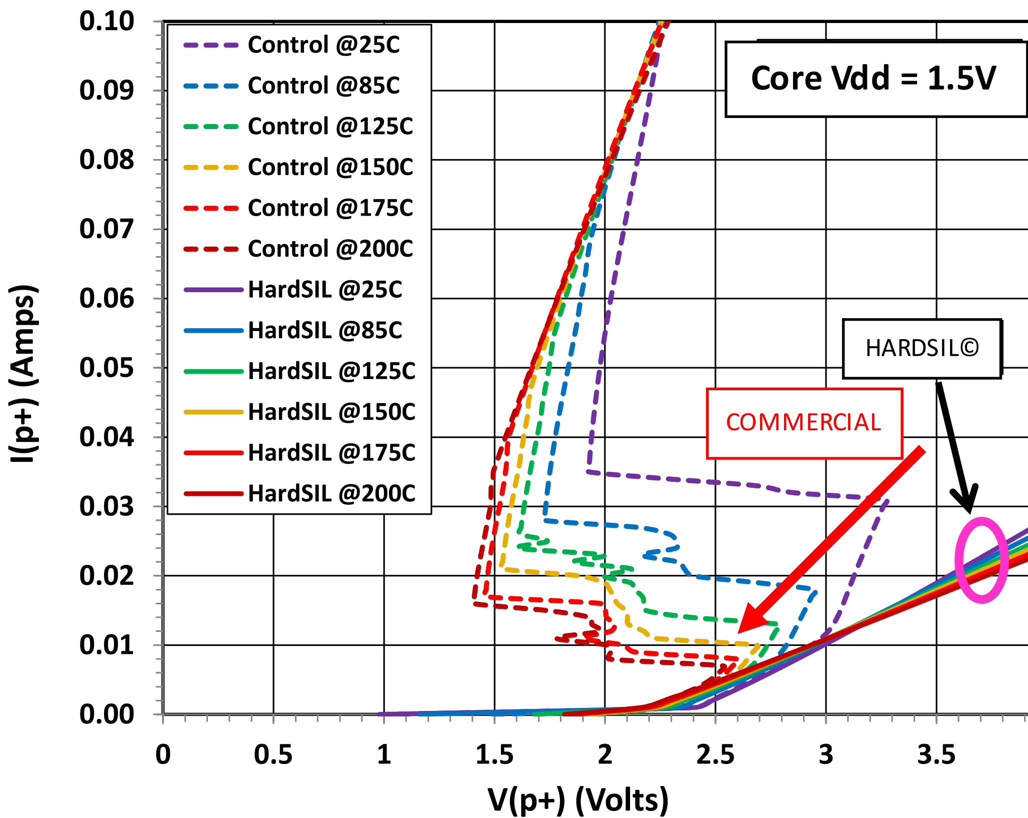
Using a commercial (130nm) CMOS process and the HARDSIL© process, two sets of latch up test structures were manufactured and latch-up characterization testing conducted across a temperature range from 25˚C to 200˚C. The latch-up data taken shows the effect of increasing temperature on latch-up trigger current for the two samples. A signal overvoltage condition is established by applying an increasing forward bias to the P+/NWL diffusion to conduct P+ emitter current to Vss (parasitic PNP collector). The latch-up testing is conducted using the same latch-up test structure (layout at 450nm N+/P+) with two different chip voltages, core VDD test at 1.5V and IO VDD test at 3.3V.

Core VDD Latch-up testing at 1.5V:

The test results indicated that as temperature increases, the trigger current is reduced for the commercial sample. In contrast the HARDSIL© latch-up test structure does not trigger into latch-up for all temperatures

across the testing range up to 200˚C. Figure 5 plots the trigger current data for the commercial process sample (dashed line) and the HARDSIL© process sample.

Figure 5 - Latch-up characterization for a 130nm commercial CMOS process vs HARDSIL process and latch-up characterization vs. temperatures (25˚C to 200˚C) at core voltage 1.5V and N+/P+ spacing of 450nm.



For the commercial core VDD latch-up test device the latch-up trigger current is reduced from 288uA to 178uA when temperature is increased to 85˚C. This is further reduced to 109uA when temperature is increased to 125˚C. The holding voltage for core device at 85˚C is 1.73V (higher than core voltage up to 145˚C), but the holding voltage is almost at 1.5V at 150˚C, which implies that a commercial core device operating at 150˚C will be at risk for destructive latch-up event if a latch-up triggering stimulus occurs in the core circuitry as the core temperature approaches 150˚C or higher. Ambient temperature plus electrical conduction within the chip will increase the junction temperature even higher than the operating ambient temperature.

The Latch-up test data also shows for CORE voltage a HARDSIL© test device does not trigger into either latch-up or micro latch-up at up to 200˚C. HARDSIL© devices are observed to be latch-up immune for the temperature range (25˚C to 200˚C) with N+/P+ spacing of 450nm.

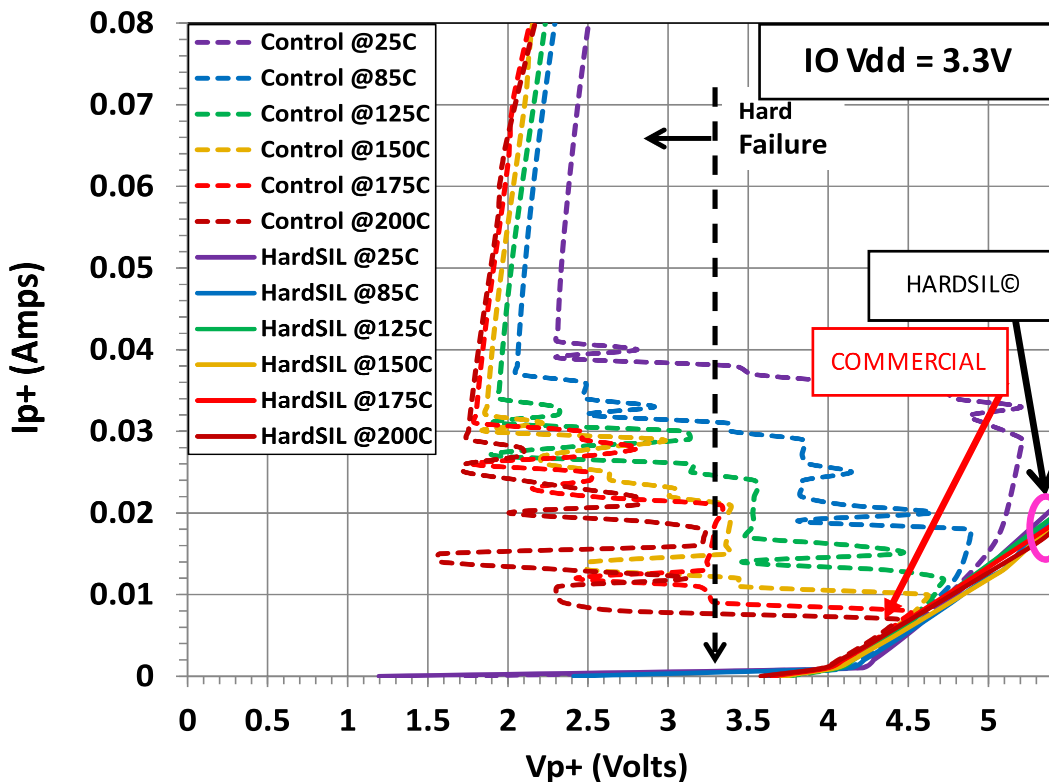
IO VDD Latch-up testing at 3.3V:

Commercial IO layout rules have wider spacing than core layout rules due to higher operating voltage of the IO at 3.3V. It is unrealistic to expect the commercial IO device to pass latch-up testing at core layout spacing with the higher operating voltage. However, latch-up characterization was performed on the HARDSIL© test device with the core layout spacing rules and the IO voltage (3.3V). The test result data in Figure 6 shows that for the commercial device, latch-up is triggered for all temperatures (25˚C to 200˚C). Therefore, it would be

impossible to use the tighter core spacing in a commercial IO device or operate at temperatures exceeding 25˚C.

In contrast, the latch-up test data for the HARDSIL© device (using the same 450nm latch-up test structures) will not trigger into latch-up or micro latch-up even at 200˚C with an applied IO voltage of 3.3V. HARDSIL© devices consistently demonstrate latch-up immune behavior even while operating in the temperature range up to 250˚C.

Figure 6 - Latch-up characterization for a 130nm commercial CMOS process vs HARDSIL process and latch-up characterization vs. temperatures (25˚C to 200˚C) at IO voltage (3.3V) and N+/P+ spacing of 450nm.



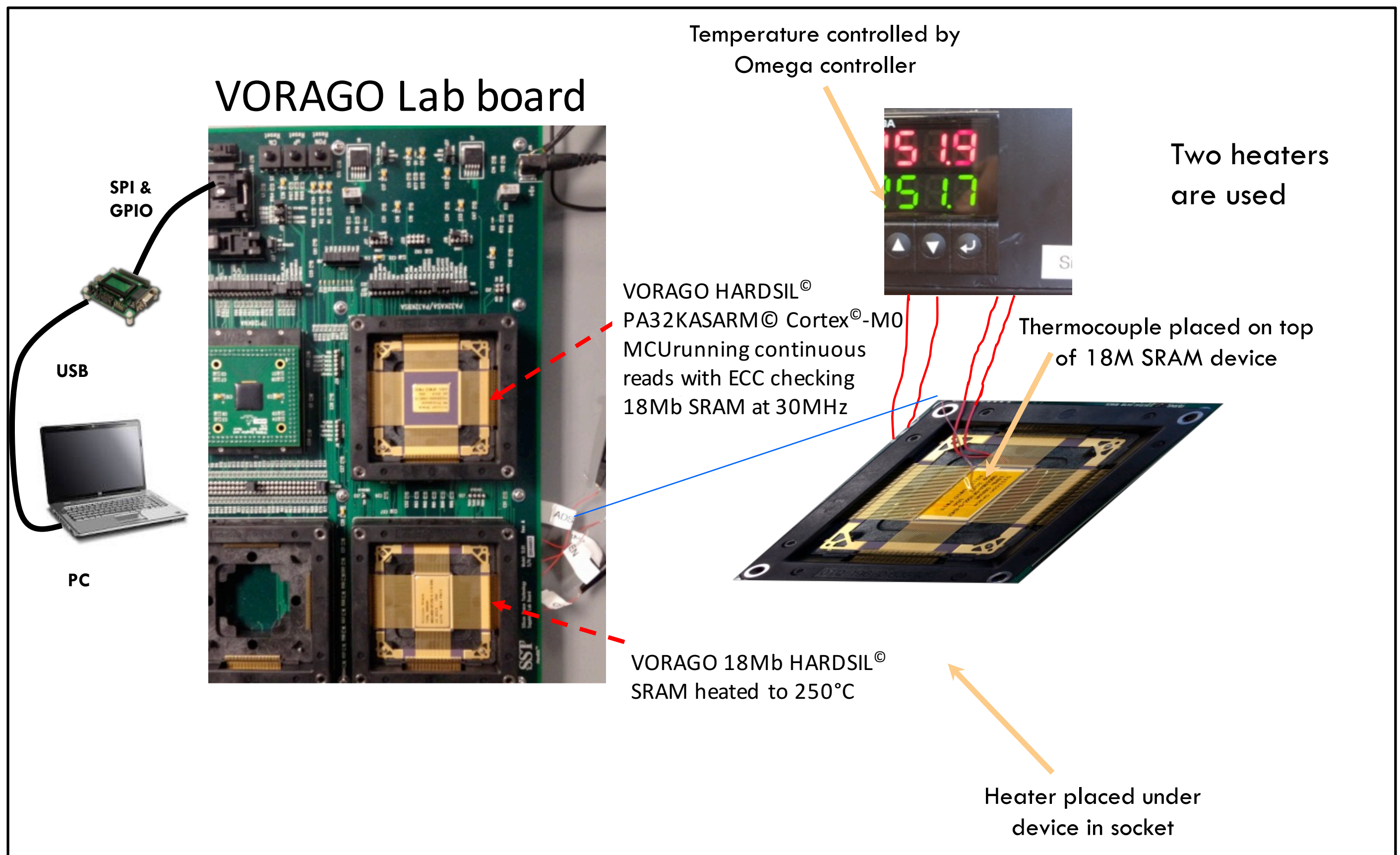
Life Testing at 250˚C on HARDSIL© 18Mb SRAM Device

A dynamic lifetime test of an 18Mb CMOS SRAM manufactured with HARDSIL© was performed at 250˚C for 2600 hours. During the life test the SRAM was cycled (daily) from 25˚C to 250˚C and clocked at 30MHz while performing read operations. Testing was stopped after 2600 hours as the board had become unusable due to the effects of prolonged high temperature exposure. The HARDSIL© SRAM DUT was still functioning normally when testing was stopped and there was no reason to suspect that it would not have continued to operate normally.

The SRAM was controlled by an HARDSIL© based ARM© Cortex©-M0 microcontroller (available from VORAGO, part number PA32KAS) performing bit error checking (ECC) on the SRAM. Figure 7 illustrates the test set up for the 18Mb SRAM. The temperature is read by two thermocouples attached to the package at

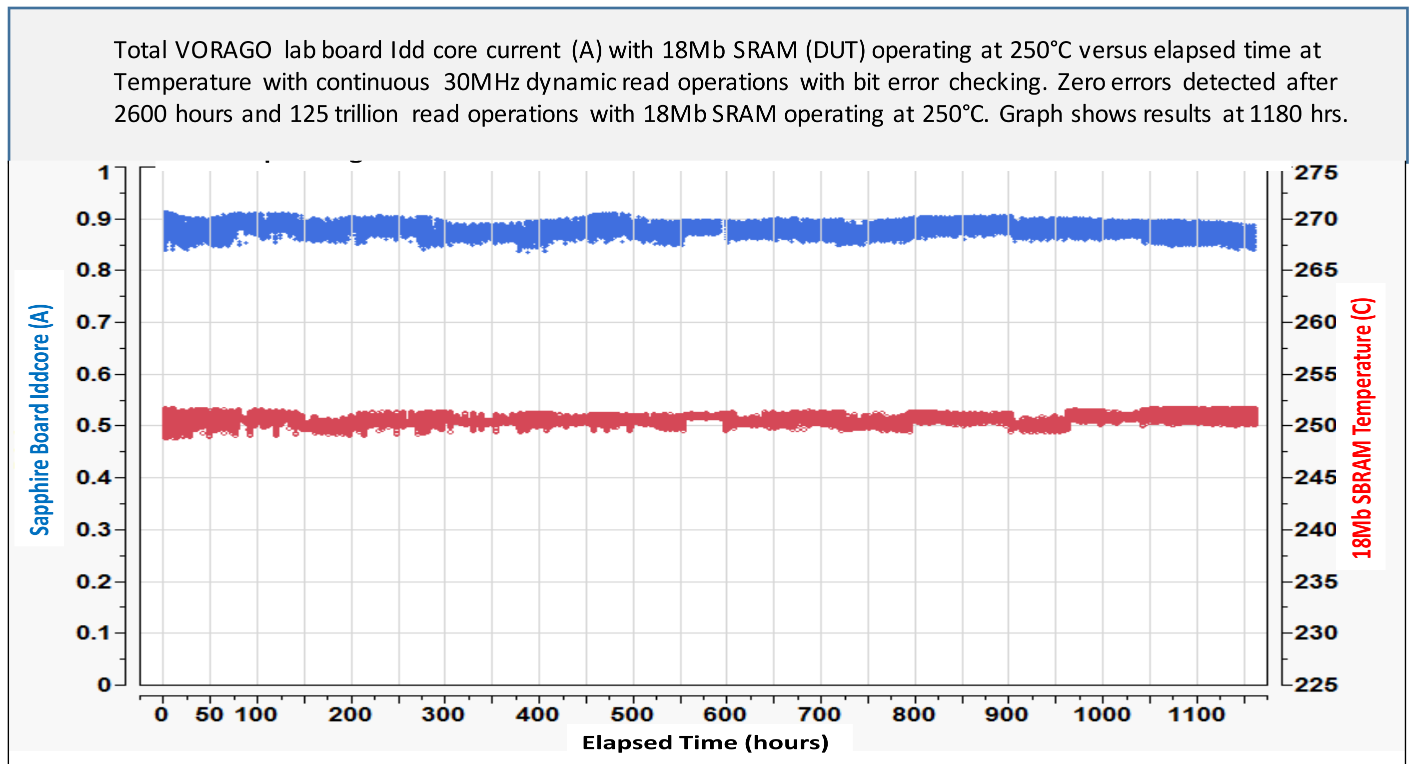
the top and bottom of the SRAM ceramic package. Heaters are separately controlled (top and bottom) by an external controller. Temperature is controlled to +/- 0.5˚C.

Figure 7 - VORAGO lab board for 18Mb SRAM HT life test. The 18Mb SRAM (DUT) is heated by strip heater from external controller.



A portion of the heat control plot of temperature v power that was maintained during the life test is shown in Figure 8 from zero to 1180 hours. Temperature is shown in red with the scale on the right hand side of the chart. Current consumption (for the entire lab board) is shown in blue with the scale on the left hand side. The operating current of the SRAM (@ 250˚C) was measured at 550mA, and did not vary throughout the test. Zero errors were detected during the 125 trillion read operations at 250˚C during the course of the 2600 hours of testing.

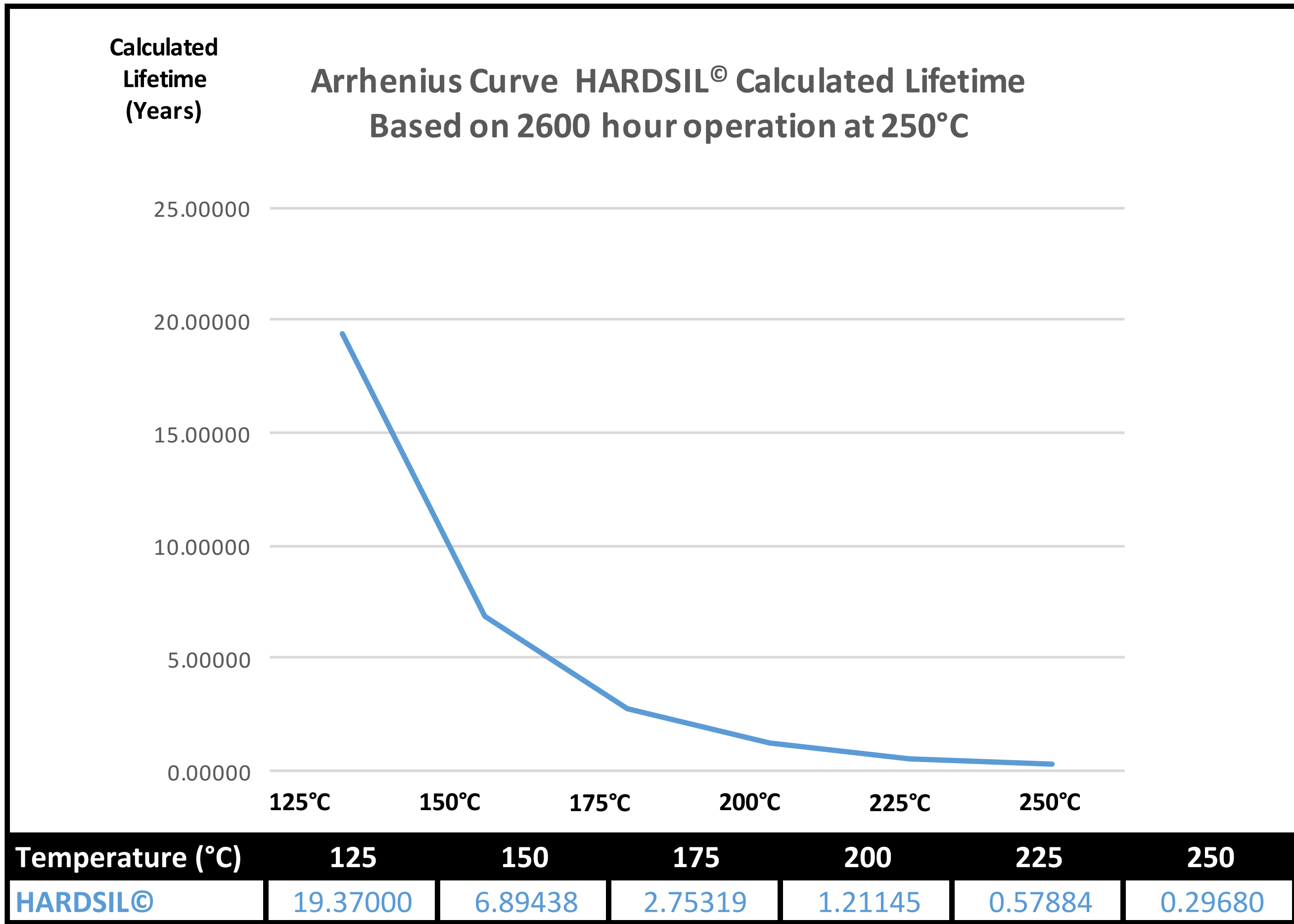
Figure 8 - Temperature and Current Consumption of 18Mb SRAM



The 18Mb SRAM was read by the microcontroller at 30 MHz continuously throughout the test. SRAM bit error checking was performed by the microcontroller with ECC located in the microcontroller. The SRAM is read in native mode (ECC is off and NOT used) during bit reads and NO error correction or write backs are performed by the controller. A different memory pattern was loaded each day before heating the SRAM. During the 250˚C life test all SRAM addresses (0 to 512K x 36) are read and checked for errors by the parity checking in controller every 5 seconds.

No bit errors, latch-up events or current drift was detected at any time during the 2600 hour life test. An Arrhenius plot of predictive lifetimes at lower temperatures was constructed and is shown in Figure 9. The Arrhenius plot predicts lifetimes of 19.37 years at 125˚C for HARDSIL© devices based on the 2600 hour exposure at 250˚C when testing was concluded.

Figure 9 - Arrhenius life time plot based on 2600 hours @ 250˚C.



Temperature (°C)	125	150	175	200	225	250
HARDSIL©	19.37000	6.89438	2.75319	1.21145	0.57884	0.29680

Summary

Latch-up is a phenomenon in all bulk CMOS devices that increases in likelihood significantly as temperature increases. The HARDSIL© Buried Guard Ring structure that is created beneath the CMOS device has proven to be effective in immunizing against latch-up.

Comparison testing has been performed using identical CMOS devices with and without HARDSIL© processing implemented. The HARDSIL© based devices were shown to be latch-up immune under elevated temperature conditions while the commercial CMOS devices latched-up.

Extended temperature testing at 250˚C on a HARDSIL© treated SRAM device for 2600 hours demonstrated no instances of memory bit errors or latch-up. In this time, 125 trillion memory reads were executed and stable current consumption was observed.

HARDSIL® technology can be integrated into any commercial CMOS process, at any CMOS generation, at any CMOS wafer fab. There is no yield impact on wafers that have had HARDSIL© implemented and there is no performance impact on the devices other than hardening against temperature effects, better ESD and noise immunity characteristics.