Innovation: Optimizing Mission Assurance on a Smallsat Budget

A VORAGO Technologies Focus

by Ross Bannatyne, Director of Marketing, VORAGO Technologies

Although cubesats are expected to be created and deployed relatively inexpensively, there are rising expectations about their reliability.

New Cubesats are expected to operate for longer, in more extreme conditions and observe controlled decommissioning. These objectives are difficult to achieve using Commercial Off-The-Shelf (COTS) electronic components that were not designed to operate in a radiation environment. Conversely, specialist rad-hard components are expensive, often unaffordable for a cubesat, or smallsat, budget.

A New Approach to Radiation Hardening

HARDSIL® technology was developed to harden standard CMOS devices against the effects of radiation. Because no specialty wafer fab or equipment is required to harden CMOS-based ICs using HARDSIL, it is possible to create chips at a lower cost than up-screening COTS devices. This brings rad-hard performance capability into the budget envelope for cubesats.

When a high-energy radiation particle strikes silicon, it leaves in its wake a stream of electron-hole pairs that should ideally recombine quickly without the stray charge upsetting any nearby transistors. Unfortunately, there is an unfriendly byproduct of building CMOS devices that results in millions of parasitic bipolar transistors being embedded in the silicon just below the transistor active areas.

These parasitic structures resemble thyristors and lay dormant unless they are triggered by an unwanted event such as a transient that results from a particle strike. *Figure 1* illustrates a side view of a commercial CMOS structure.

There is an NMOS transistor on the left, a PMOS transistor on the right and the circuit diagram of the parasitic bipolar thysistor structure is superimposed on the diagram. If stray charges from a particle strike cause the parasitic transistors to become forward biased, a short circuit will be created from VDD to VSS. This condition is known as latch-up and requires a reset to rectify — in some cases latch-up can destroy the device.

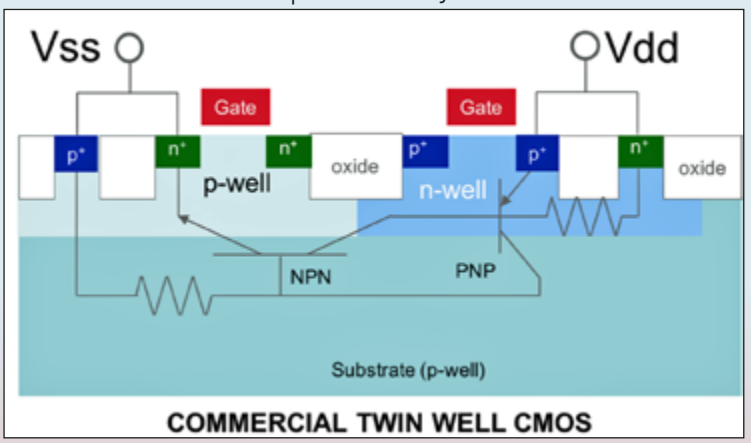
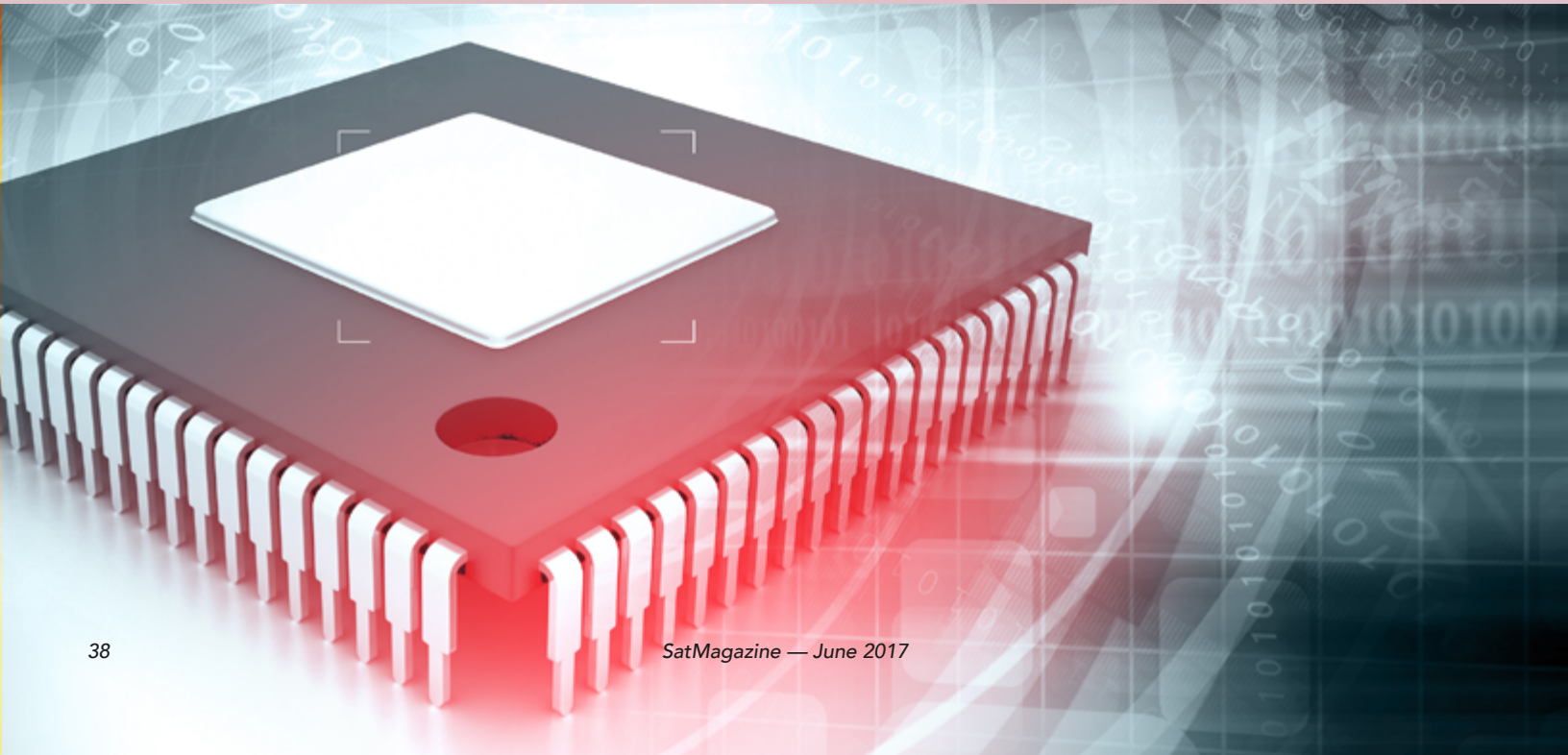


Figure 1. A commercial twin well CMOS device with parasitic thyristor structure.

One of the benefits of HARDSIL technology is to prevent radiation-induced latch-up. This is accomplished by modifying the standard CMOS processing flow in a few simple steps to



implant a 'Buried Guard Ring' (BGR) in the substrate just below the active transistor areas. The BGR prevents the parasitic bipolar transistors from triggering by ensuring that stray charges cannot forward bias them. The HARDSIL® implant is shown in *Figure 2*. The BGR implant is located in the substrate below the CMOS devices. The layers of metal that make up the die can be seen above this area.

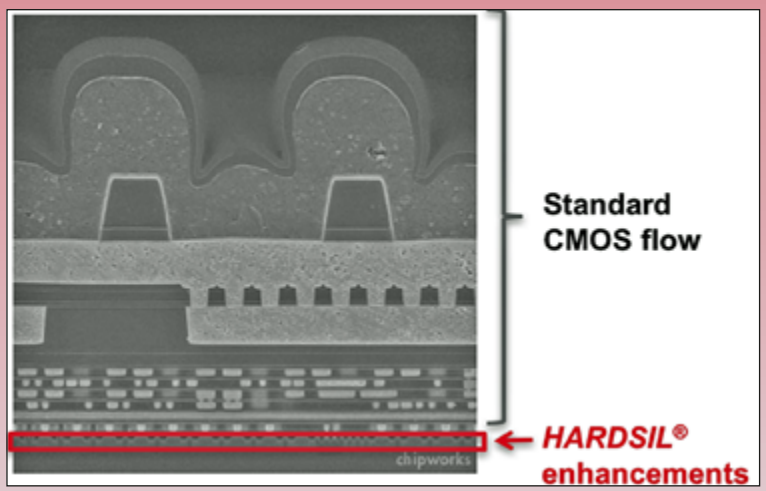


Figure 2. HARDSIL® Buried Guard Ring modification to CMOS device.This approach to hardening silicon against the effects of radiation and preventing latch-up is cost-effective because it piggybacks on workhorse semiconductor industry CMOS processes and can be implemented easily. Because it doesn't follow traditional Rad-Hard-by-Design methodologies, it doesn't rely on inefficient spacing between structures or using redundant devices to safeguard the circuits.

Products for Cubesats

HARDSIL technology has now been implemented by different semiconductor suppliers on a range of different products for space and other harsh environment applications. VORAGO Technologies have developed ARM® Cortex®-M0 microcontrollers for the purposes of providing a rad-hard option for cubesats / smallsats. The VA10820 microcontroller includes additional on-chip features to protect the device against Single Event Upsets (SEU) that can result in flipped memory bits without inducing latch-up. A block diagram of the VA10820 is shown in *Figure 3*.

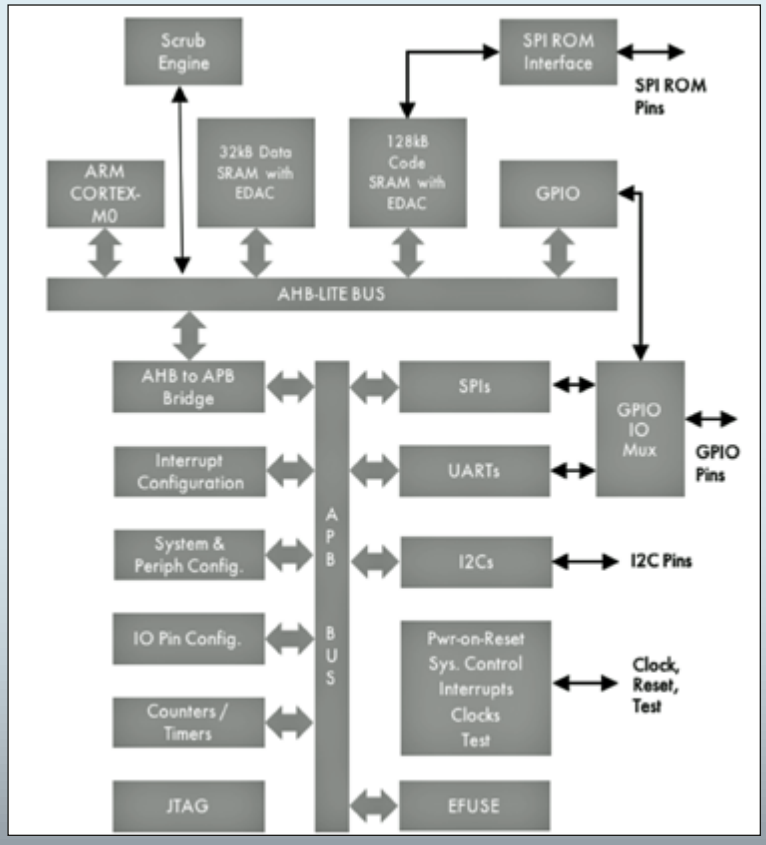


Figure 3. Block diagram of rad-hard A10820 microcontroller.

An Error Detection and Correction (EDAC) subsystem is built into the memory block. When the CPU fetches a 32-bit word, the subsystem inspects it on a byte level to detect up to two errors and correct one error per byte.

To reduce the probability of two flipped bits occurring within a single byte (which would be considered an uncorrectable error) a Scrub engine is used in conjunction with the EDAC. The Scrub engine is used to sequentially step through all memory locations in the memory map, checking for flipped bits and correcting them before the CPU fetches them. This is an effective approach to ensure that data that is infrequently accessed by the CPU / EDAC mechanism gets 'scrubbed' for errors.

The frequency of the Scrub operation is flexible and can be increased if there is a higher level of radiation activity — this would be apparent if the EDAC were to indicate that a flipped bit was observed.

In addition to on-chip memory protection for SEUs that can disrupt memory contents, there are hardware circuit features integrated to protect logic circuits. These techniques are similar to conventional approaches in high-reliability systems and include Dual Interlocked storage CEll (DICE) latches, Triple Modular Redundancy (TMR) on critical registers and clock glitch filtering.

Onwards and Upwards

The good news is that there is now technology within reach that addresses the need for reducing the risk of mission failure at a reasonable cost. This technology is operating today on the International Space Station and is enabling many upcoming smallsat missions.

In recent years, cubesats have contributed significantly to commercial enterprise projects and space science. Success rates must continue to improve, but at a cost that is affordable to continue the momentum. The availability of affordable rad-hard components will be a key enabler to maintain this progress.

Ross has spent his career in semiconductors in Silicon Glen, Silicon Valley and Silicon Hills (Scotland, San Francisco Bay Area and Austin, Texas). He is the author of books and patents relating to microcontrollers and enjoys following Glasgow Celtic Football Club and the Oakland Athletics.