Latchup Immunity in High Temperature Bulk CMOS Devices

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ABSTRACT

High density, low power 180nm and 130nm CMOS SRAMs have been manufactured on bulk silicon wafers using a modified CMOS commercial process that hardens the junction isolation and has demonstrated latchup immunity at temperatures >200˚C. TCAD simulations confirmed by high temperature testing indicate that a latch up free performance of SRAMs manufactured on bulk silicon modified by the *HardSIL*™ technology will easily extrapolate to 250˚C. These process modifications result in significantly more robust CMOS circuits making them more suitable for highly reliable operations in extreme environments – such as radiation and high temperature. The unique capability of *HardSIL*™ technology to enhance existing IC products has demonstrated excellent results with several commercial circuits. This new approach enables the conversion of commercial off the shelf (COTS) circuits to hardened hi-rel commercial circuits with dramatically improved survivability to either radiation or high temperatures. Latchup immunity has been demonstrated on two high-density bulk silicon CMOS SRAMs: a 16Mbit asynchronous SRAM manufactured at the 180nm design node and an 8Mbit dual port synchronous SRAM manufactured at 130nm. Both parts were produced in a high-volume, low-defect commercial CMOS fabrication facility in the USA. The SRAM parts were packaged in ceramic packages and characterized at temperatures ranging from 25˚C to 225˚C. Characterization data indicates both excellent static leakage and dynamic circuit performance for both SRAMs at these elevated temperatures. Device test structures designed with typical layout spacing rules were evaluated to quantify latchup and isolate the various leakage mechanisms. Detailed results for these test structures are presented and compared to the SRAMs using the modified *HardSIL*™ process.

INTRODUCTION

Multiple high reliability or mission critical electronic market segments including oil and gas exploration and production, aerospace, automotive, medical devices, and energy generation rely on sophisticated integrated circuits which are increasingly needed to operate in higher temperature environments. Significant gaps in multiple electronic component categories still persist for these high temperature market segments some six years after conducting an initial survey [1]. High temperature electronic applications require unique technical solutions and design considerations for survivability and for complying with other critical performance metrics such as low operating power budgets and latch-up immunity. The limitations of bulk silicon CMOS technology for high temperature operation have been reviewed previously [2, 3, 4, 5]. These limitations, namely latchup and excessive leakage, have been broadly verified relegating bulk CMOS devices to temperature operation typically below ~100˚C. As a result, alternative materials such as silicon on insulator (SOI) and silicon carbide (SiC) have been explored and successfully deployed for elevated temperature applications [2, 6, 7]. While offering the fundamental advantage of latch-up immunity at elevated temperatures, SOI- and SiC-based designs suffer from the limited IP portfolio of parts, and when available, are generally much larger geometry devices. This precludes the use of most commercially available, high performance CMOS circuits; circuits highly desirable by engineers who seek increased processing power, memory, etc.

While these high-performance bulk CMOS ICs are abundantly available, these COTS devices are limited to temperature operation <85˚C and are typically not suitable for high temperature environments such as down hole drilling (DHD). However, complex engineering workarounds for certain critical high temperature applications have been developed including extensive up-screening and testing, specialized packaging, and localized cooling. These factors, coupled with the inherent device physics limitations of the isolation properties of bulk silicon devices, limit the broad adoption of bulk CMOS devices for high temperature applications.

SST has introduced a novel approach called *HardSIL*™ which can provide latchup immunity and excellent leakage performance in devices for high temperature applications >200˚C by making astute modifications to the commercial CMOS manufacturing process to improve junction isolation. Having proven the radiation hardness of the technology across several CMOS manufacturing nodes (250nm, 180nm, and 130nm) and different bulk CMOS devices for the radiation-rich environment of space, this paper's objective is to report on the same hardening benefits of the *HardSIL*™ technology for high temperature environments. The technology has been successfully demonstrated in two SRAMs operating at high temperatures (>200˚C) providing technical proofs for wider use of this modified bulk CMOS technology in high temperature products. Exploitation of the full portfolio of existing, high performance CMOS devices without the need for circuit redesign or the complicated engineering workarounds mentioned above would greatly enable the high temperature industry.

We have chosen to develop hardened high density SRAM memories as our initial product offering due to their broad application. Many high temperature electronic applications make use of various memory devices to store the data generated, move the data from one location to another for processing, or provide configuration files for critical on-board processors. In down hole drilling applications, the need for more real-time intelligence and more comprehensive data collection is driving an unprecedented amount of enhanced processing and associated memory. To that end, this paper will focus on the high temperature characterization of our high density SRAMs and the TCAD modeling to characterize the electrical characteristics. Measurements described herein demonstrate that the *HardSIL*™ technology can extend bulk CMOS high temperature reliability and survivability to at least 200˚C and with expected extrapolation, to 250˚C or higher.

CMOS LATCHUP

The greatest risk for high reliability CMOS circuits is latchup. The basic switching circuit is the inverter composed from a complementary pair of MOS transistors, one NMOS and the other PMOS (Figure 1).

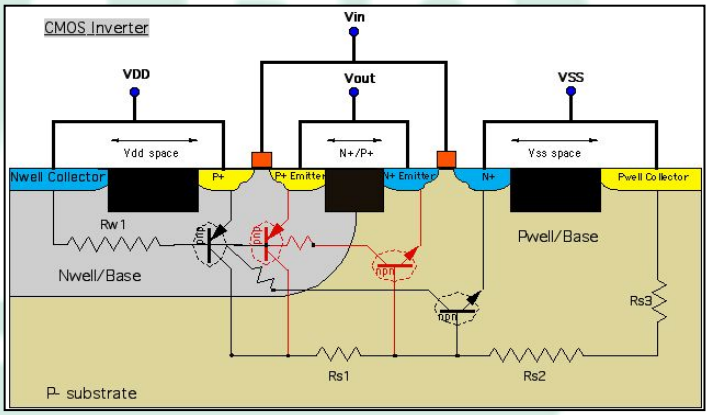

Figure 1: CMOS inverter showing bipolar parasitics.

Electrical isolation is achieved from both dielectrics and from p-n junction diodes. However, the CMOS twin well structure also contains a parasitic resistor/bipolar transistor network which can be biased into a high current, low impedance state. This state is known as latchup, and it can physically destroy the silicon integrated circuit if not properly mitigated. The network of series resistors shown in Figure 1 can allow the local potentials to stray from their intended values as defined by the electrode biases, allowing the structure to trigger into this latchup state [8, 9]. The latchup state is characterized by significant potential drops across both the Nwell and Pwell parasitic resistances, forward biasing of the emitters of both the parasitic NPN and PNP devices, and collapse of the Nwell/Pwell junction. It can be triggered by a random ionizing event such as an ion strike, or it can be caused by a voltage spike on any of the

electrodes. This latter path to latchup is simulated on a latchup structure shown in Figure 2. Figure 3 shows the p+ current as the p+ electrode boundary conditions are swept. Key features are the trigger current and trigger voltage as defined by the rightmost point of the trace, and the holding voltage as defined by the leftmost point on the high-current, or latched part of the trace. Increasing trigger current and increasing trigger voltage indicate decreasing probability of accidentally moving into the latchup state. A holding voltage less than the supply voltage allows the latchup state to be sustained indefinitely, and possibly destructively. Even a transient triggering event can be disruptive enough to cause the upset of a large region of CMOS circuit, compromising either memory or logic. This ability of a latchup event to spread in area is demonstrated in the next simulation.

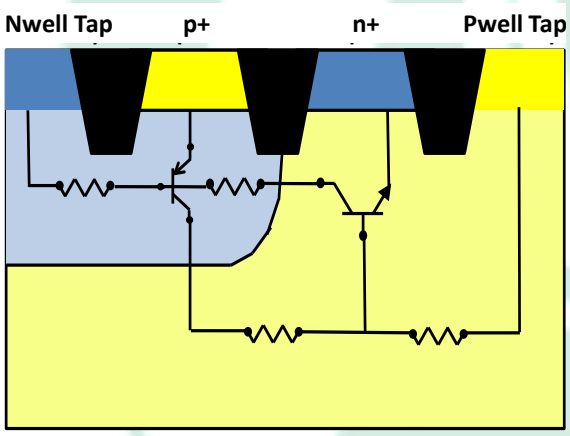

Figure 2: Latchup test structure showing the parasitic resistor/bipolar transistor network.

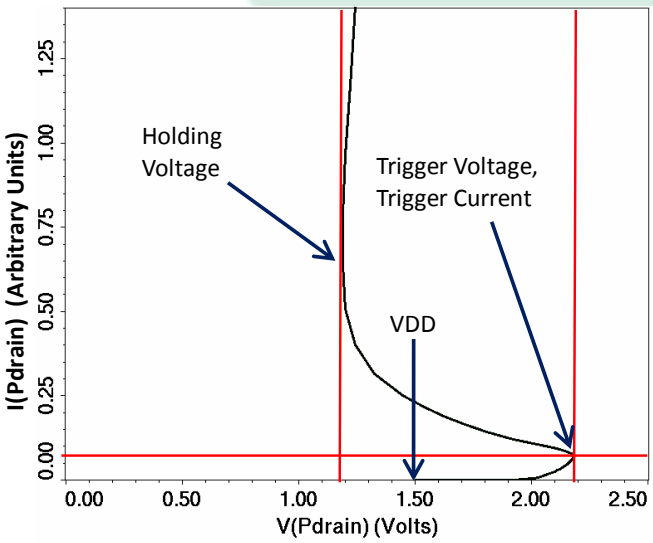

Figure 3: Latchup current vs. voltage.

Figure 4 shows a simulation of two inverters after latchup was induced by tracing the right PMOS drain as described above. The current flow lines indicate both total current direction and total current density with 3% of the total current flowing between each pair of adjacent flow lines. The interesting point here is that large currents flow not only on the right side of the simulation, but also on the left side, to where the latchup event has spread via collapse of the well junction. Figure 5 shows this evolution of the currents for each of the silicon nodes vs. PdrainR (drain of PFET on right side) voltage. Simulations on the *HardSIL*™ variant of this 2-inverter structure show no sign of latchup up to five volts on PdrainR (Figure 6).

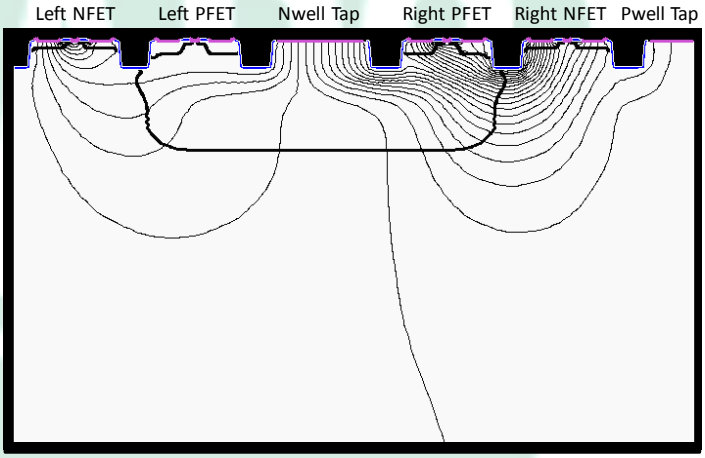

Figure 4: Device simulation of two inverters in a latched state. The thick lines indicate junctions, and the thin lines indicate current contours.

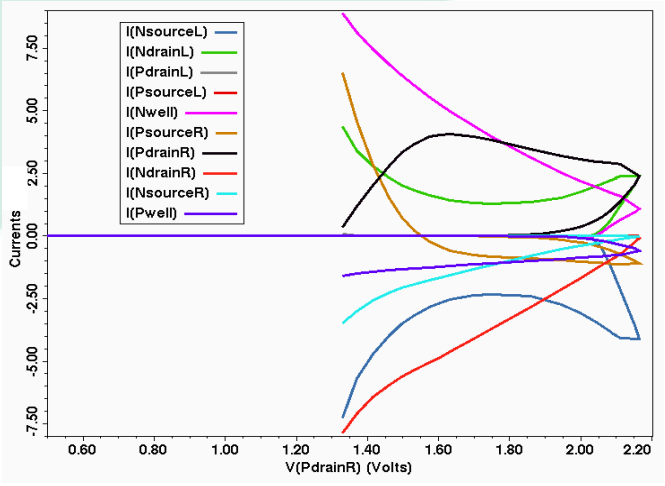

Figure 5: Terminal currents (arbitrary units) in the two-inverter simulation (control). The boundary conditions of PdrainR are stepped.

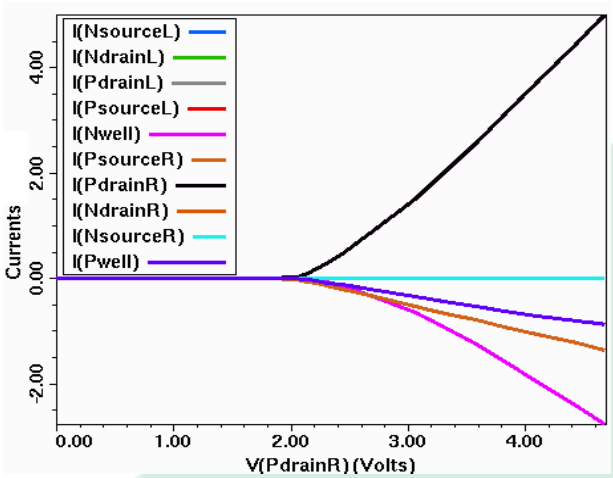

Figure 6: Terminal currents (arbitrary units) in the two-inverter simulation (*HardSIL*™).

LATCHUP MEASUREMENTS

If the trigger and holding voltages can be made so high that devices would first break down through other mechanisms such as gate oxide failure, then for all practical purposes the latchup state does not exist. With the high integration at these technology nodes, this is the simplest way to ensure that latchup cannot occur anywhere on the circuit.

Latchup structures in the 130nm technology node were drawn and tested. The measured structures are the same as shown in Figure 2, with the minimum spacing rules, and a width of 20μm in the z-direction. By applying a voltage sweep at the P+ diffusion the PNP devices is activated and latchup traces were taken for both the control and *HardSIL*™ cases at temperatures up to 200˚C (Figure 7). The control case went into a latched state at all temperatures; with decreasing trigger current, trigger voltage, and holding voltage as the temperature was increased. At 175˚C and above, the holding voltage has dropped below the supply voltage of 1.5 V, indicating that if the overvoltage stimulus was removed the latched state could be sustained. However, none of the *HardSIL*™ cases latched, nor was there any indication that they would have even if higher temperatures had been tested beyond the equipment test limit of 200˚C. In fact, the simulations of these same structures, which agree well with the measurements of Figure 7, indicate no sign of latchup up to 275˚C.

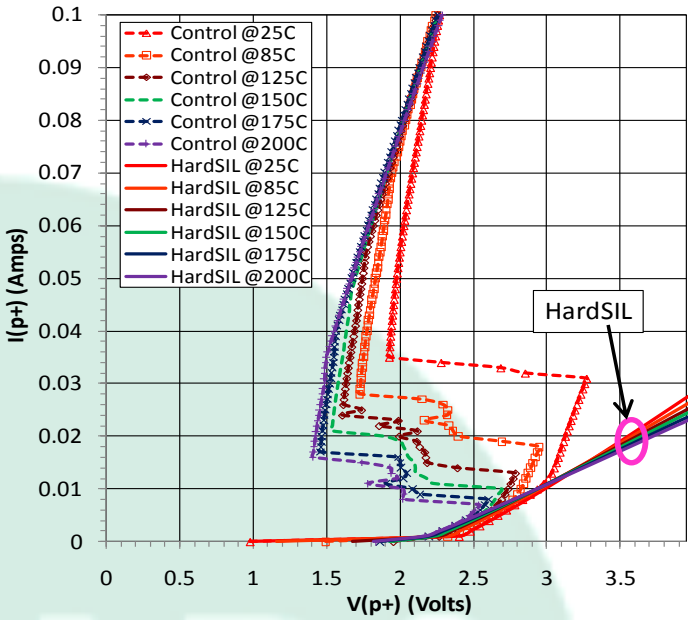

Figure 7: Measured currents from a latchup test core devices. The temperature is stepped to 200 ˚C for both the control and *HardSIL*™ cases.

This same structure, with the minimum Nwell edge spacing ground rules for core devices, was further stressed by increasing the V_{DD} voltage from 1.5V to 3.3V as is used in the I/O devices. Normally, I/O devices need about three times the minimum allowed spacing rules to the Nwell edge to prevent latchup. As seen from Figure 8, latchup occurs in the control case and is prevented in the *HardSIL*™ case. This suggests that the *HardSIL*™ technology can be used to improve the trade-off between layout ground rules/total area and the assurance of latchup prevention. Because latchup in the I/O has been a big concern historically, the approach with *HardSIL*™ has been to retain the established ground rules to gain the added security against latchup.

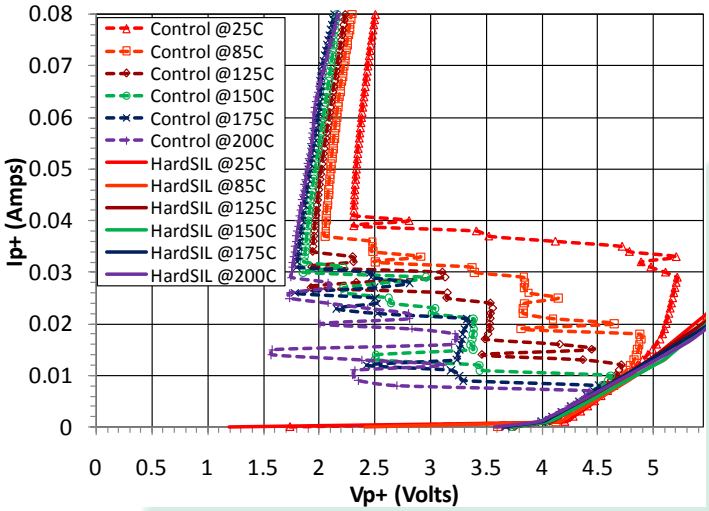

Figure 8: Measured currents from the latchup test device with V_{DD}=3.3V. The temperature is stepped to 200 ˚C for both the control and *HardSIL*™ cases.

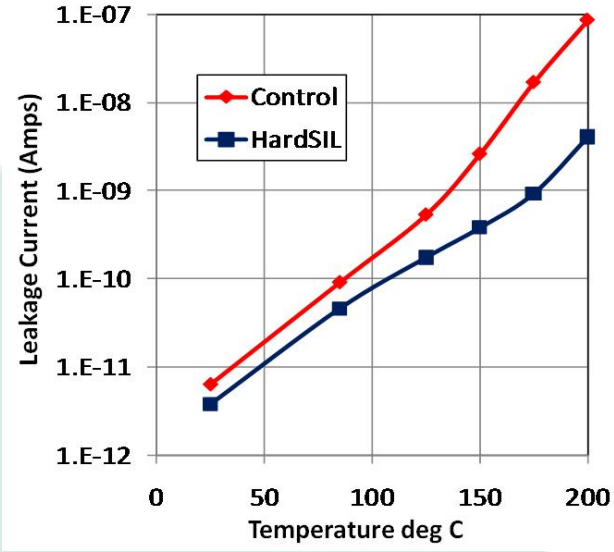

Figure 9: Measured averaged Nwell-Psubstrate junction leakage currents vs. temperature (˚C). The drawn Nwell area is 503 µm².

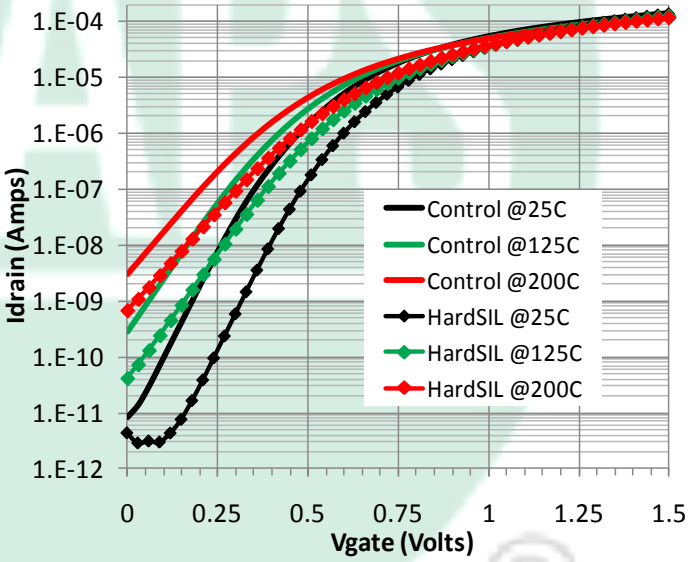

Figure 10: Gate current sweeps of control and *HardSIL*™ NMOS core transistors (L=115nm, W=250nm) at the 130nm CMOS technology node.

LEAKAGE

There are several mechanisms through which unwanted current can leak from V_{DD} to ground: junction leakage through the reverse-biased drains and through the reverse-biased Nwell-Psubstrate junctions, NMOS-Pwell or interdevice leakage along a shallow trench, or intradevice source-to-drain leakage. The *HardSIL*™ process changes reduce junction leakage, particularly the Nwell-Psubstrate leakage which is reduced by more than a factor of ten at 200˚C as shown in Figure 9. The Ndrain leakage is also reduced, but by a much smaller factor. However, the largest contribution to overall leakage in these highly integrated digital CMOS circuits is source-to-drain current in the CMOS transistors themselves—either under the gate according to the basic subthreshold characteristics, or along the edge, assisted by charge traps in the oxide near the interface. The *HardSIL*™ technology has been used to specifically reduce NMOS source-drain leakage, mainly to prevent increased leakage from TID (Total Ionizing Dose) in radiation environments. As shown from measured data in Figure 10, there is also significant leakage reduction at high temperature, without radiation.

For example, the control and *HardSIL*™ I_{on} currents at 200˚C are within 3% of each other (1.16e-4 Amps and 1.13e-4 Amps respectively), yet the *HardSIL*™ devices have smaller I_{off} by a factor of 4.3 (2.93e-9 Amps and 6.77e-10 Amps, respectively).

SRAM HIGH TEMPERATURE TESTING

Two different SRAM memory products have been fabricated with the *HardSIL*™ technology. A 16

Mbit SRAM at the 180nm technology node, and an 8 Mbit dual-port SRAM at the 130nm node. For these full parts, as opposed to structures on a test chip, "full" control cases were not fabricated because that would have involved expensive layout differences. This section concentrates on the performance of the *HardSIL*™ SRAM parts themselves. Figure 11 shows plots of I_{DD1} stand-by current and read current for the 16 Mbit SRAM at temperatures from 25˚C to 225˚C. Above 200˚C, the leakage current is comparable to the read and write currents. Figure 12 shows leakage current of the 8 Mbit dual-port SRAM vs. temperatures from 25˚C to 225˚C. In both SRAMs, *HardSIL*™ acts to limit leakage and as can be seen up to 225˚C, the leakage increases in a log normal fashion. Additional high temperature characterization and testing of *HardSIL*™ parts will continue in order to establish survivability metrics, statistically validate electrical performance, etc.

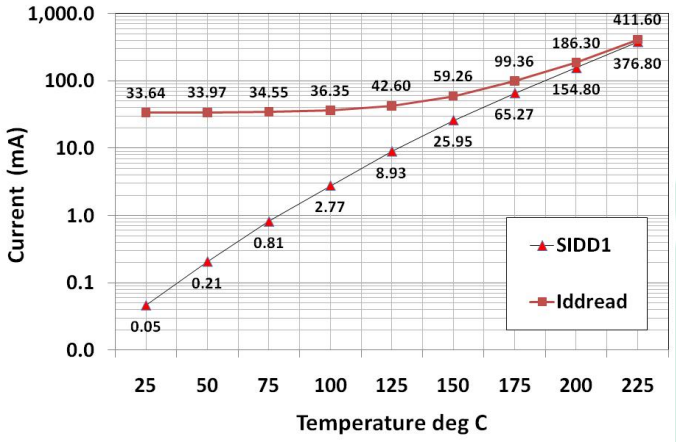

Figure 11: 180nm 16M SRAM SIDD1 and 5Mhz read current vs. temperature.

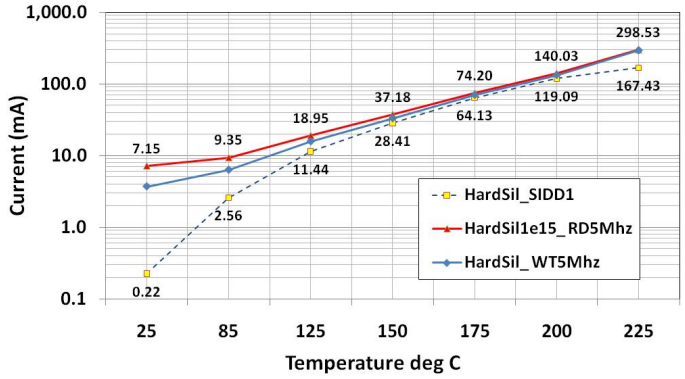

Figure 12: 130nm 8M SRAM SIDD1 and 5MHz read, write currents vs. temperature.

Summary

Commercial off the Shelf (COTS) bulk CMOS IC's are generally not optimized for high temperature use. *HardSIL*™ represents a new approach to hardening the CMOS process technology used to manufacture CMOS IC's and has been proven to prevent latchup even while operating at temperatures >200˚C. SOI technology has long been the "incumbent solution" for high temperature applications requiring latchup free performance with reduced leakage performance relative to traditional bulk CMOS. However, the results published here provide compelling evidence that *HardSIL*™ offers a viable high temperature alternative to SOI which would increase the availability of high performance, HT-CMOS devices due to the large IP portfolio and existing circuit designs used in COTS. Upgrading existing bulk silicon devices by manufacturing them with the *HardSIL*™ process will greatly expand the availability of components operating reliably at temperatures >200˚C. This modified bulk CMOS process offers a new, high performance hi-rel solution with latchup immunity for T>200˚ and lower leakage relative to conventional bulk CMOS technology.

REFERENCES

[1] Normann, Randy A., "First High-Temperature Electronics Products Survey 2005", Sandia Report SAND2006-1580, 2006.

[2] Colin Johnson and Alison Crossley, "High Temperature Electronics in Geothermal Tools", HITI Final Paper, 16-17, Sept. 2010.

[3] Patrick McClusky, Richard Grzybowski, Thomas Podlesak, editors, "High Temperature Electronics", CRC Press, 1997.

[4] B.L. Gingerich, SPE, and P.G. Brusius, "Reliable Electronics for High- Temperature Downhole Applications," 1999 SPE Annual Technical Conference and Exhibition, Houston, Texas, 3-6 October 1999.

[5] Pect, Micheal. "The Influence of Temperature on Integrated Circuit Failure Mechanisms.", Quality and Reliability Engineering International, May-June 1992, Vol. 8, No 3, pp.167-175.

[6] Bruce Ohme and Michael T. Johnson, "Deep Trek Re-configurable Processor for Data Acquisition (RPDA)", Final Report, DOE Award No.: DE-FC26-06NT42947, Sept. 2009.

[7] L. Evans, "High Temperature Electronics for Intelligent Harsh Environment Sensors", PWIG Workshop, May 2008.

8] R. Troutman, "Latchup in CMOS Technology: The Problem and the Cure," Kluwer Publications, Ch. 6 and 7, 1986.

[9] S. Voldman, "Latchup," ISBN: 987-0-470-01642-8, Feb. 2008.