Hardening of Texas Instruments' VC33 DSP

Robert Fuller, Wesley Morris, David Gifford, Rex Lowther, Jon Gwin, James Salzman, David Alexander and Ken Hunt

***Abstract*—A hardened version of Texas Instruments' VC33 Digital Signal Processor was created without any mask changes. The commercial mask set was processed using Silicon Space Technology's HardSIL™ process variant to produce the hardened version. Radiation testing of the resulting hardened circuit demonstrated significant improvement in performance.**

I. Introduction

SILICON Space Technology (SST) was awarded a SBIR Phase II contract by MDA in April 2008 to manufacture a hardened version of Texas Instruments' (TI) VC33 Digital Signal Processor (DSP). The approach for producing a radiation-hardened 250nm VC33 incorporates SST's proprietary HardSIL™ techniques for improving circuit performance in extreme environments. In the Hard*SIL*™ approach, radiation-hardening process modules were introduced into TI's commercial 250nm (VC33) CMOS process flow. This approach, depicted in Fig. 1, allows existing off-the-shelf commercial circuits to be radiation hardened without circuit redesign. Additionally this approach enables the design and production of custom ASIC's using the same layout rules and standard cell libraries used in commercial circuits. Hardening is achieved by manufacturing the ASIC with the Hard*SIL*™ modified process. This manufacturing approach allows maximum circuit packing density and low power; and it minimizes the circuit area, power, performance and cost penalties normally associated with a Radiation Hardened-by-Design approach. Key to the Hard*SIL*™ approach is that it provides a solution for all radiation environments both natural and man-made. Hard*SIL*™'s minimally invasive hardening methods [1], [2]; previously shown to address Total Ionizing Dose (TID), Single-Event Effects (SEE), and Dose Rate (DR); are demonstrated again in the VC33 catalog DSP COTS part manufactured by TI. No circuit design, layout, or package changes were made to achieve radiation hardening of the VC33. The exact same standard commercial design was simply run through TI's 250nm CMOS process augmented by SST's Hard*SIL*™ process modules. Radiation testing has shown that TID, DR and SEE performance are significantly improved in the VC33 DSP manufactured with the Hard*SIL*™ modified process.

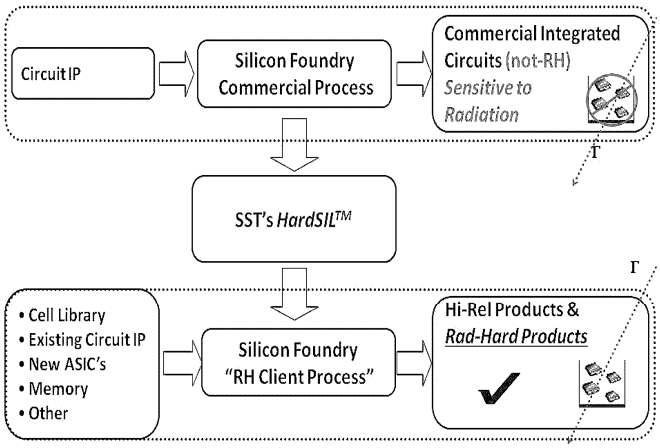

Fig. 1. SST manufacturing model at a commercial foundry with Hard*SIL*™™ process enhancements added to create a radiation-hardened silicon process – the "RH Client Process."

II. Description of the VC33 DSP

The TMS320VC33 DSP is a 32-bit, floating-point processor manufactured in TI's 250nm four-level-metal CMOS technology. The TMS320VC33 is part of the TMS320C3x generation of DSPs from Texas Instruments. The TMS320C3x's internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 150 million floating-point operations per second (MFLOPS). The TMS320VC33 optimizes speed by implementing functions in hardware that other processors implement through software or microcode. The TMS320VC33 can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The TMS320C3x supports a wide variety of system applications from host processor to dedicated coprocessor. High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible

Manuscript received Match 10, 2010. This work was supported in part by the U.S. Missile Defense Agency under SBIR Phase II contract W9113M-08-C-0163

R. Fuller, W. Morris, D. Gifford, R. Lowther and J. Gwin are with Silicon Space Technology, Austin, TX 78738 USA (telephone: 512-347-1803, e-mail: rfuller@siliconspacetech.com).

J. Salzman is with Texas Instruments, Sherman, TX 75090 USA. (telephone: 214-538-5086, e-mail: salzman@ti.com).

D. Alexander was with the Air Force Research Laboratory, Albuquerque, NM 87117 USA, now retired).

K. Hunt is with the Air Force Research Laboratory, Albuquerque, NM 87117 USA

instruction set, and well-supported floating-point arithmetic. The TMS320VC33 has 1 Mb of on-chip SRAM.

III. Test Procedure

A. Test Hardware

A J/D Instruments ATV tester was used to evaluate device performance during radiation tests. J/D Instruments was also contracted to build the test board and develop the test program for the tests.

The J/D Instruments tester connects via three meter cables to a test head. A test board to hold the device under test (DUT) is then either plugged directly into the test head, or extension cables (up to one meter in length) can be used to separate the test board from the test head. The test-head-to-test-board extension cables limit the frequency at which the DUT can be operated, so these extender cables were only used when the test environment required the test board and test head to be physically separated.

In all tests, the tester was placed behind appropriate shielding to protect the sensitive electronics in the tester from irradiation. In tests where the directionality of the radiation was not controllable (i.e. TID and dose-rate tests) extender cables were used between the test board and test head to allow shielding of electronics within the test head.

The J/D Instruments tester is controlled using a laptop computer connected to the tester through USB. USB distance limitations combined with long distances between control and source/target rooms at the test facilities required additional hardware to allow the controller computer to interface with the tester over the required distances. A Black Box Remote Port USB 2.0 → CAT5 Port Extender was employed to increase maximum allowable distance between the tester and computer controller to 50 meters. Most radiation test facilities provide CAT5 Ethernet cables between the control and source/target chamber; so the USB → CAT5 port extender was a perfect solution. A diagram of the hardware set up is shown in Fig. 2.

B. Test Software

Testing DSPs and microprocessors using general IC testers has been problematic in the past due to the complexity of these devices. DSPs are actually integrated systems and subsystems with many additional IC technology types embedded as internal "peripherals." Previously the specialized requirements of these parts has led to testing approaches that made dynamic upset and some in-situ testing abstract – potentially missing many failures. Often design or application programs and vectors were run during test to create a pass/fail type test, rather than create programs that specifically separate out and test the various sub-system components. This did not give insight into the processor failure levels, mechanisms, and modes [3], [4].

For testing of the VC33 DSP, the ATV test software was enhanced to make testing of microprocessors and DSPs a single step, completely inclusive solution. Specifically, the ATV technology was advanced so that a processor's assembly level "instruction set" can be programmed directly in the ATV environment.

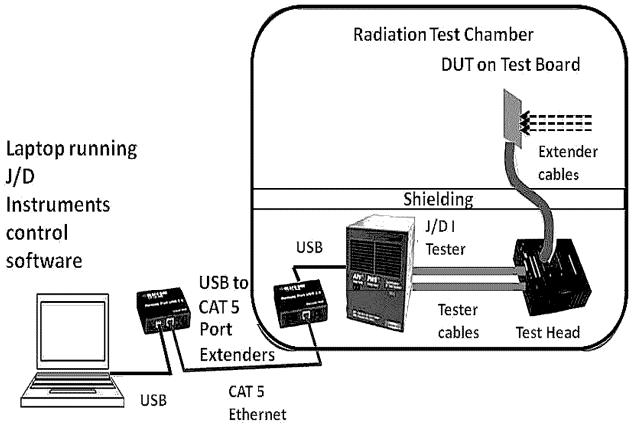

Fig. 2. Typical radiation test set up

In this way a program was created to isolate the DSPs major subsystems for independent test (to the extent possible).

In general, the approach was to first create a test where only the Program Control circuitry (PC) of the DSP is exercised. Since the PC is involved in operating other subsystems, its failure levels provide a "baseline" for the part. In other words, the radiation sensitivity of other subsystems can only be differentiated if they are more susceptible to radiation than the PC portion. Based on previous experience it was expected that the PC circuitry would be the most radiation resistant portion of the parts because its circuitry is usually fairly simple, being composed mainly of control circuitry and registers.

After the PC failure level was established, separate test programs were exercised to test other individual subsystems including:

embedded RAM,
embedded registers,
ALU, and
CPU.

IV. Total Dose Testing Results

Testing was performed using the Cobalt 60 gamma-ray system at the Air Force Research Laboratory facility on Kirtland AFB, NM. The test boards were constructed so multiple samples could be irradiated and measured in situ. Samples from two process splits were measured: control parts which were not processed through the hardened steps and the hardened parts which included the hardened process steps. The parts were irradiated with a checkerboard (CB) pattern stored in the internal memory and the standby current was measured with the checkerboard pattern and the inverse checkerboard pattern in memory after irradiation. The devices were also tested for PC (basic function), CPU, and ALU functionality. The control parts exhibited a rapid increase in standby current for TID > 50 krd(Si). After TID = 100 krd(Si), the worst-case standby current for the controls was 500 mA. The controls also exhibited memory failures starting

at 75 krd(Si) and memory plus functional fails at 100 krd(Si). In contrast the hardened split significantly outperformed the control parts. Hardened parts exhibited a much slower increase in standby current. After TID = 1 Mrd(Si), the worst-case standby current was 70 mA for the hardened process with the checkerboard (CB) pattern stored in the array. Fig. 3 shows the control and hardened Device-Under-Test (DUT) standby current vs. TID curves with CB patterns. No functional or memory fails were observed for the hardened part. It should be noted that the standby currents for the checkerboard and inverse checkerboard patterns were similar when measured after irradiation for all samples.

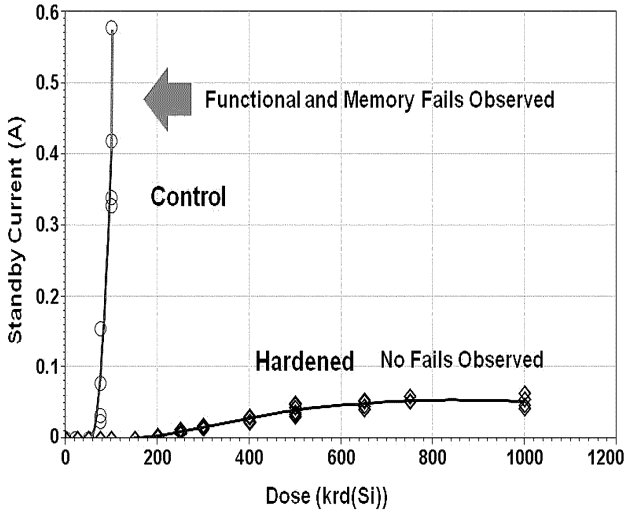

Fig. 3. Standby current as a function of total dose for the hardened and the control samples. The hardened sample showed no functional failures after 1 Mrd(Si) where the control sample failed after less than 100 krd(Si).

A second set of tests was performed in the gamma cell to determine the effect of gamma cell dose rate on total dose performance. These results are shown in Fig. 4. The post-irradiation standby currents for the control parts show no direct correlation to the gamma cell dose rate. The hardened parts show a clear correlation with reduced standby current after 200 krd(Si) as the dose rate is reduced. Fig. 5 shows the relationship between the current after 200 krd(Si) and dose rate is approximately linear and suggests that the standby current for the hardened samples will not shift at the dose rates encountered in most orbits.

V. Dose Rate Testing Results

Testing was performed using the flash x-ray system at the Air Force Research Laboratory facility on Kirtland AFB, NM. Commercial grade VC33 DSPs (control samples) exhibited single bit memory upset at 3.57×10^9 rd/s and CPU dynamic upsets at 7.77×10^9 rd/s. However, no latch-up was observed for the commercial VC33 at the highest dose rate.

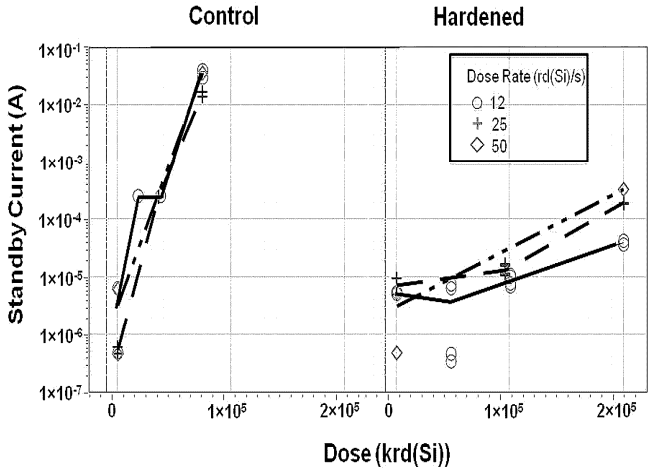

Fig. 4. Standby current vs. TID as a function of dose rate for control and hardened samples. The standby current for the hardened samples decrease with dose rate. The current is unaffected by the dose rate for the control samples.

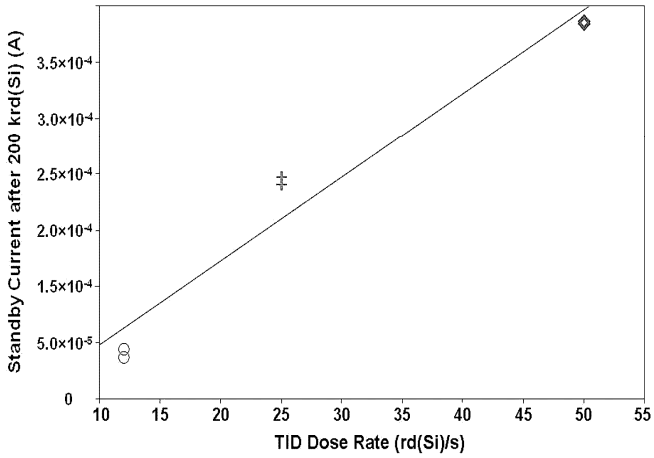

Fig. 5. Standby current after 200 krd(Si) vs. TID dose rate for the hardened parts. The increase in current post radiation decreases linearly with the dose rate, suggesting little or no change at the dose rates in most orbits.

In contrast, neither single bit upsets nor CPU errors were observed for the hardened samples up to the highest dose rate achievable in the flash X-Ray system (1.73×10^{10} rd(Si)/s). As expected the hardened parts also did not latch up at the highest dose rate. As shown in Fig. 6, the hardened parts showed an improvement of over five times in dose rate hardness from the commercial parts.

VI. Single Event Test Results

A. Single Event Upset

Testing was performed using the cyclotron at Texas A & M University (TAMU). Many tests were run to test the various components of the DSP. As would be expected the on-chip memory showed the most sensitive and largest cross-section. Figure 7 shows a linear Weibull fit of the memory upsets vs. LET. While the onset LET is similar for both samples, the plot shows that the hardened parts have lower native cross-section at higher LETs.

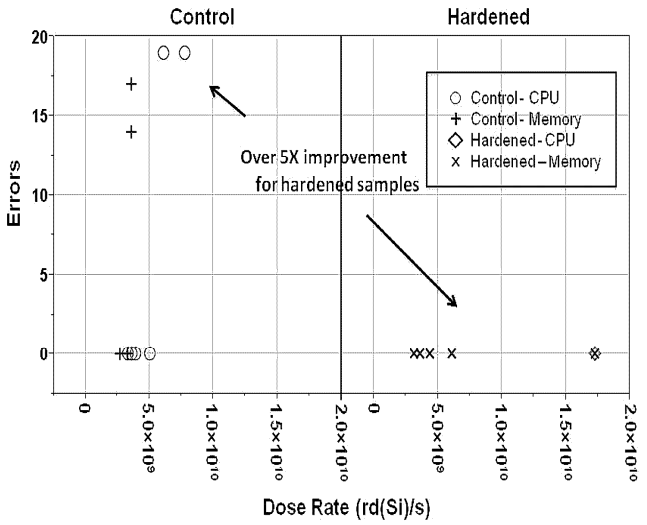

Fig. 6. Dose rate testing results showing no errors for the hardened part at the maximum achievable dose rate.

This has previously been shown to be due to the charge coupling effect leading to the higher occurrences of large MBUs (multiple-bit upsets) with control parts vs. the hardened parts [5].

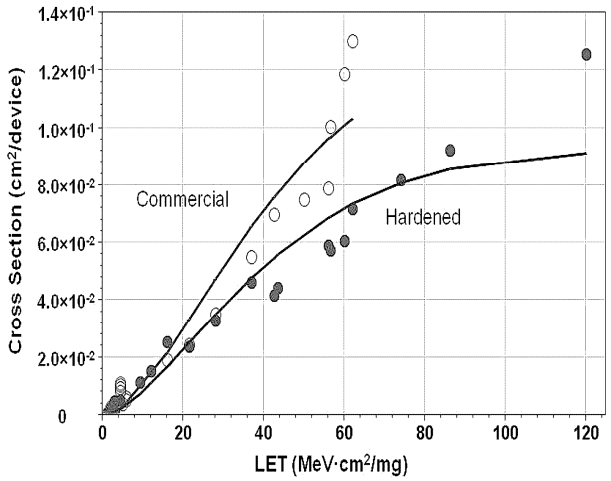

Fig. 7. Device cross sections and Weibull fits as a function of effective LET for the VC33 DSP memory. While the onset for both samples is similar, the saturation cross section is lower for the hardened device. The cross section for both parts deviated significantly from the Weibull fit at high LET's.

Multiple tests were conducted; similar curves were derived for the various other DSP subcircuits; and each curve was fitted with a Weibull function. The resulting coefficients were entered into the CRÈME96 software and the error rates for a geosynchronous orbit at a solar minimum were calculated. These results are summarized in Table I. The hardened part's memory error rate is improved by over 25% from the control parts; and these errors are many times more frequent than are the errors in the other DSP subcircuits

B. Single Event Latch-up Test Results

The samples were tested for single-event latch-up by exposing the sample to a fluence of 1×10^7 ions/cm^2. The supply current was monitored to determine if latch-up had occurred. Table II shows a summary of the observed latch-up behavior. At temperatures above 85^0 C the control parts latched at an LET of 21.5 MeV-cm^2/mg. At room temperature the control samples latched at LET's of 74 MeV-cm^2/mg and above. In contrast the hardened VC33 DSPs did not show any latch-up even at an LET = 125 MeV-cm^2/mg while operating at a temperature of 150˚C and an overvoltage of 10% (1.98 V).

TABLE I
SUMMARY OF ERROR RATES FOR VC33 SUB-CIRCUITS

Test	Sample	SEUs/bit/s	SEUs/device/s	Device Days/Error	Average Years before error
ALU	Control	5.14×10^{-10}	5.14×10^{-10}	2.25×10^{4}	61.7
ALU	Hardened	4.28×10^{-10}	4.28×10^{-10}	2.70×10^{4}	74.1
Basic Function	Control	9.24×10^{-10}	9.24×10^{-10}	1.25×10^{4}	34.3
Basic Function	Hardened	8.98×10^{-10}	8.98×10^{-10}	1.29×10^{4}	35.3
CPU	Control	9.79×10^{-10}	9.79×10^{-10}	1.18×10^{4}	32.4
CPU	Hardened	1.12×10^{-9}	1.12×10^{-10}	1.03×10^{4}	28.2
Memory	Control	3.95×10^{-12}	3.95×10^{-6}	2.93	0.0
Memory	Hardened	2.91×10^{-12}	2.91×10^{-6}	3.98	0.0
Registers	Control	6.87×10^{-9}	6.87×10^{-9}	1.68×10^{3}	4.6
Registers	Hardened	8.29×10^{-9}	8.29×10^{-9}	1.40×10^{3}	3.8

TABLE II
SUMMARY OF LATCH-UP TEST RESULTS

Test	Ion	Angle (deg)	Effective LET (MeV-cm^2/mg)	Temp. (° C)	Vdd Core (V)	Control Sample Latch?	Hardened Sample Latch?
CPU 25MHZ	Kr	0	21.5	125	1.8	Yes	No
CPU 25 MHZ	Kr	0	21.5	100	1.8	Yes	Not Tested
CPU 25 MHZ	Kr	0	21.5	85	1.8	Yes	Not Tested
CPU 25 MHZ	Kr	0	21.5	70	1.8	No	Not Tested
Register Test	Kr	60	74	25	1.8	Yes	No
ALU	Kr	60	74	25	1.8	Yes	No
Basic Func	Xe	60	86.3	25	1.8	Yes	No
CPU 3 MHZ	Xe	60	86.3	25	1.8	Yes	No
CPU 25 MHZ	Xe	60	86.3	25	1.8	Yes	No
ALU	Xe	60	125	125	1.98	Not Tested	No
ALU	Xe	60	125	150	1.98	Not Tested	No

The 25MHZ CPU test was the most sensitive to latch-up, especially at the higher temperatures. Latch-up was observed for others tests on the control part. No latch-up was observed for the memory test.

VII. Summary

SST has demonstrated hardening of a commercial DSP without any design or mask changes. TI's commercial 250nm VC33 DSP was hardened using SST's HardSIL™ techniques. The circuit demonstrated robust die yield at first silicon. The hardened VC33, radiation tested for DR, TID, and SEE, shows the following achievements:

DR threshold exceeding 1.7×1010 rads(Si)

TID performance of ~1Mrad(Si) with no bit or functional fails and < 70mA post radiation ISB.

A 2x improvement (reduction) in SEU cross-section at high LET

Complete elimination of SEL at LET> 125 MeV-cm2/mg while the circuit was operating at 150˚C and at 10% over voltage.

VIII. Acknowledgment

Silicon Space Technology thanks David Sleeter and Jake Tausch of J/D Instruments for their considerable effort in developing test hardware and software for this project. We also thank Jake Tausch for his assistance in the testing of the parts.

IX. References

[1] W. Morris, R. Lowther, D. Alexander, J. Gwin, "Buried Guard Rings as a Solution to Single-Event Effects," Hardened Electronics And Radiation Technology (HEART) Conference, March, 2007.

[2] W. Morris, R. Lowther, J. Gwin, "Application of the Parasitic Isolation Device (PID) into a 180nm Commercial CMOS Process to Achieve Megarad TID Hardening," Hardened Electronics And Radiation Technology (HEART) Conference, March, 2007.

[3] Kinnison, J.D.; Maurer, R.H.; Carkhuff, B.G.; Conde, R.F.; Buchner, S.P.; Kang, K.; Stapor, W.J.; Campbell, A.B.; Herlich, G.A.; Moore, H.C., "Radiation characterization of the ADSP2100A digital signal processor," *IEEE Trans. on Nucl. Sci.*, vol. 39, no. 3, , pp. 1398 - 1402, Dec. 1991.

[4] Harboe-Sorensen, R.; Seran, H.; Armbruster, P.; Adams, L., "The single event upset response of the Analog Devices, ADSP2100A, digital signal processor," *IEEE Trans. on Nucl. Sci.*, vol. 38, no. 6, , pp. 441 - 445, June. 1992.

[5] Robert Fuller, Wes Morris, Jon Gwin, Rex Lowther, Dave Gifford, Paul Young, "Performance of SST 16Mb SRAM," Hardened Electronics and Radiation Technology (HEART) Conference, April, 2009.