

# High temperature / radiation hardened capable ARM® Cortex®-M0 microcontrollers

R. Bannatyne, D. Gifford, K. Klein, C. Merritt  
VORAGO Technologies  
2028 E. Ben White Blvd., Suite #220,  
Austin, Texas, 78741, USA.  
Ph: 512-347-1800  
Email: marketing@voragotech.com

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## Abstract

VORAGO Technologies has developed a pair of ARM Cortex M0 MCUs designed from the ground up to be high temperature capable. One of these devices is specifically developed for high temperature applications, the other adds capabilities that make it suitable for use in high radiation environments as well. These devices are fabricated using a modified version of commercial bulk 130nm CMOS technology utilizing our HARDSIL® technology, which provides immunity to the increased effects of latchup and EOS encountered at higher application temperatures. In addition to the processor these devices include features more typical of low temperature SoCs including on-chip memory, timers, and communications peripherals. In addition to the ceramic package and die format typically utilized at high temperature, a new lower-cost plastic package is available that has been characterized at higher temperatures. These devices have been characterized at temperatures up to 200C and results showing the latchup behavior and device performance are provided. Some of the tradeoffs involved in creating such devices are discussed, as well as some of the similarities and tradeoffs in creating a radiation hardened devices vs. a high temperature device.

## Key words

Extreme, High-temperature, Microcontroller, Rad-hard, Reliability, MCU.

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## I. Introduction

Today there are limited choices available to a designer of embedded systems that require operation under extreme temperature or radiation conditions. In most cases, a legacy product that has been up-screened will be used. Often a device such as a DSP or FPGA will be used on account of their availability as an up-screened option, rather than a modern microcontroller that has been designed specifically for extreme environment operation. Engineers can usually solve the same problem with different programmable devices, but there is a trade-off in complexity of design, number of additional components required, power consumption and the ability to re-use the software that was created. In addition, the ARM® Cortex®-M core implementation opens up a vast ecosystem to the designer to simplify the design process with state-of-the-art development tools and a huge software base.

The availability of ARM® Cortex®-M based microcontrollers that have been specifically designed to

operate in extreme environments will allow designers of extreme-environment embedded systems to optimize their system design without having to compromise with many painful trade-offs. That was the driving factor behind developing the VA10800 extreme-temperature and the VA10820 radiation-hardened microcontrollers.

## II. HARDSIL® Technology

The foundation technology that is used to enable operation under extreme conditions is VORAGO's patented HARDSIL® technology. HARDSIL® is implemented with a limited change to the processing steps of standard CMOS processing. Operation in extreme environments is guaranteed by design.

Traditional CMOS processes are known not to handle radiation, extreme temperature or voltage fluctuations well due to parasitic devices that are created across the active devices and wells that form CMOS circuits. When strong

electro-migration due to high temperatures or an ionizing charge is deposited as a result of a radiation particle strike, these parasitics can result in disruptions of circuit behavior. The parasitic device in a commercial twin well CMOS circuit is shown in Figure 1.

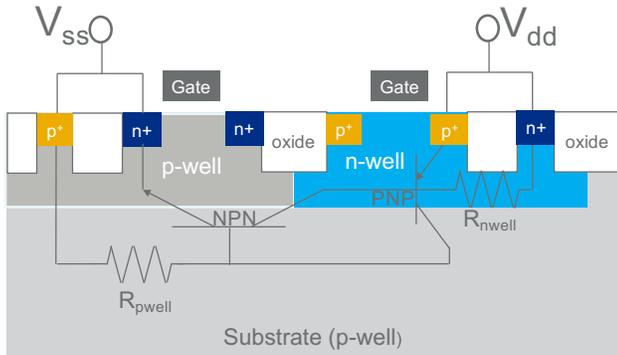


Figure 1 – Parasitic device in commercial twin well CMOS

HARDSIL<sup>®</sup> works by depositing a highly conductive layer underneath the CMOS devices and wells along with a highly conductive interconnect to the well contacts. This acts as a collection plate that reduces substrate resistance. This is shown in Figure 2 and the structure is known as a ‘Buried Guard Layer’. There is no impact on circuit performance or manufacturing yield.

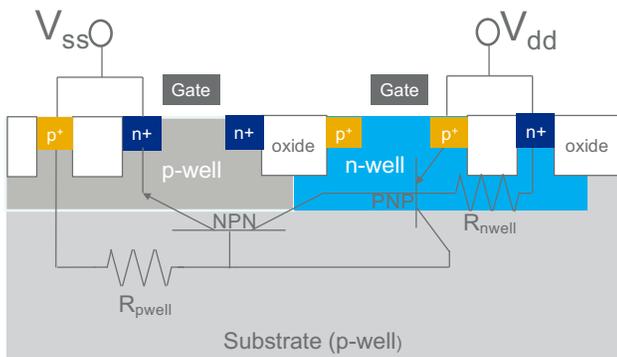


Figure 2 – Buried guard layer in HARDSIL<sup>®</sup> technology

Latch-up is eliminated from devices that have HARDSIL<sup>®</sup> by lowering the resistance of  $R_{pwell}$ . This creates a path to ground for the current flowing through the parasitic PNP transistor, such that the parasitic NPN transistor can never switch on. The  $\beta$  (gain) of the parasitic NPN device is adjusted by HARDSIL<sup>®</sup> processing to be lowered to a level that the behavior of the parasitic transistor pair cannot support latch-up. A simple diagram of the transistor pair to illustrate this is shown in Figure 3.

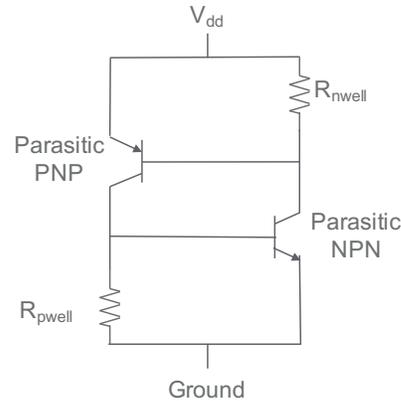


Figure 3 – Simplified diagram of parasitic transistor pair

### III. VA10800 and VA10820 microcontrollers

Both microcontrollers, the VA10800 and the VA10820 have been manufactured in CMOS using the HARDSIL<sup>®</sup> enhanced process. There are some differences between the microcontrollers in terms of both the on-chip peripherals and the process that was used.

The VA10800 was designed to operate from  $-55^{\circ}\text{C}$  to  $200^{\circ}\text{C}$ . Because of the extreme temperature that the device is subjected to, there are some additional proprietary process tweaks (or advanced transistor engineering) that are implemented in addition to HARDSIL<sup>®</sup>. These tweaks serve to address the high levels of electro-migration that can occur at elevated temperatures and ensure that operation is guaranteed by design and latch-up cannot occur. The modifications do not introduce any performance penalties (50MHz specification is met very comfortably) and improve leakage so that power consumption is also optimized. High operating temperature by-design, as implemented in the VA10800, offers several benefits over up-screened commercial off-the-shelf (COTS) devices including elimination of costly workarounds such as specialized packaging and localized cooling.

The VA10820 was designed to operate in radiation environments and is specified to withstand a Total Ionizing Dose (TID) of 300K rad (Si). This specification measures the amount of ionizing radiation that can be imparted into the silicon without causing a fault condition. There is an on-chip Error Correction and Detection (EDAC) subsystem that in conjunction with a Scrub Engine can detect flipped memory bits and correct them autonomously in real-time. When the EDAC and Scrub Engine on the VA10820 are enabled (with the SCRUB rate set fast enough to prevent accumulation of errors over time in the SRAM array for the targeted radiation environment), the upset rate is  $< 1e-12$  uncorrectable errors / bit / day (Geosynchronous orbit solar min. with 100 mils of Al shielding). A Single Event Upset

(SEU) is a change of state caused by one single ionizing particle striking a device. The specification guaranteed by VORAGO Technologies for the VA10820 (using EDAC and Scrub Engine) is *best-in-class* among programmable devices. A further enhancement in the VA10820 architecture is the implementation of Triple Modular Redundancy (TMR) on all internal registers. A block diagram of the VA10820 device is shown in Figure 4.

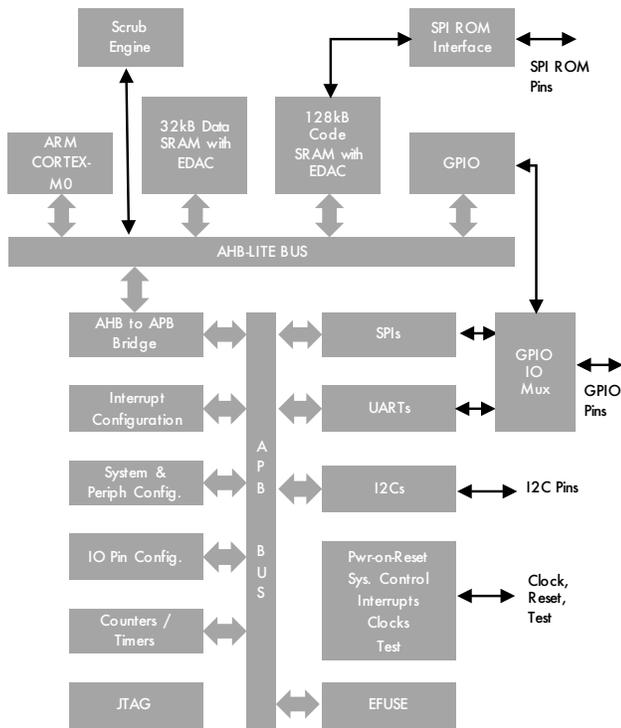


Figure 4 – VA10820 block diagram

The VA10820 microcontroller is supported with a development kit (REB1) that incorporates memory, clock, power supplies, sensors and connectors to all chip I/O. A board support package (BSP) is also supplied with example code for all peripherals.



Figure 5 – VA10820 Development Board (REB1)

#### IV. EDAC and scrub engine

The combination of an Error Detection and Correction (EDAC) module and Scrub Engine are used on the VA10820 microcontroller to ensure data and instructions read from internal memory as expected and to correct them if they are not. This is intended to fix bits that may have flipped due to an ionizing particle strike or other random upset event back to their correct state. The soft error rate of the memory cell itself (without EDAC & Scrub) is  $1.3e^{-7}$  errors / bit-day. With the inclusion of EDAC (and with scrub enabled at an appropriate rate for the anticipated radiation environment to prevent the accumulation of errors over time) will result in an uncorrectable error rate as low as  $1.0e^{-15}$  errors / bit-day.

The EDAC on the VA10820 is always on and cannot be disabled. The EDAC logic will read both the data and additional information stored in dedicated EDAC memory bits to detect single bit upsets and correct the data for use by the system. EDAC on the VA10820 is implemented at the Byte level. The EDAC memory bits are physically located in the same array as the memory words. During the VA10820 power on sequence the entire memory space is initialized to a known state so that every address starts out with a clean state.

Because there are five EDAC bits for every byte in the internal 32 bit data word, it is possible to detect 2 bit errors per byte read and correct 1 bit for each byte of the 32-bit memory word. This allows for the correction of up to 4 bit errors (one per byte) per 32 bit data word. The decision to use five parity bits for each memory byte was made for two reasons. It allows seamless support for byte-write (ability to overwrite data in memory in byte level chunks) found in modern controllers, and it provides as a good trade-off between the size of the memory array and the speed of read/write access from/to internal memory.

The EDAC is used to inspect the contents of data being read from a location from within the controller’s internal memory, and when a correctable error is detected correct the error in the information for use by the microcontroller. The EDAC Engine provides the added ability that when it detects a correctable error it automatically “writes-back” the corrected data into the memory address that was just read, effecting an immediate ‘scrub’ of the detected bit upset so that future accesses to that address will not have to correct for the error every time the data is read. To prevent accumulation of bit errors over time in the array (especially in locations seldom read) the programmable scrub engine can be activated to periodically step through the entire internal memory (both code and data spaces) reading every address at a fixed frequency and correcting bit upsets as located. The scrub operation only corrects upset(s) in one 32 bit data word per scrub cycle. An internal counter keeps

track of the next address to scrub. The scrub engine is designed to perform its duties transparently in the background providing unhindered access of the data stored in internal memory by the microcontroller. Note: it is possible (using the built in heart beat oscillator) to maintain scrub operation even when the rest of the system is in a low power idle mode. This ensures that the memory contents can be regularly ‘serviced’ for possible errors even when the system is sleeping.

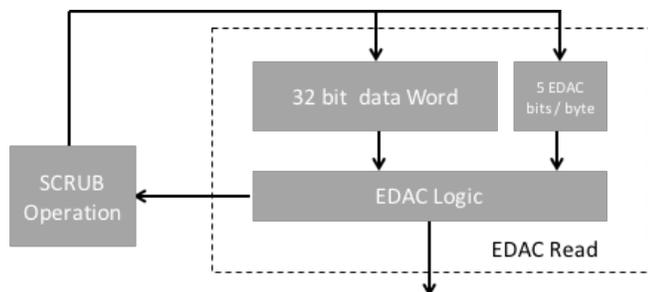


Figure 5 – EDAC and scrub engine configuration

## V. Triple modular redundancy (TMR)

Triple modular redundancy or Triple mode redundancy is used in the registers on the VA10820 to protect information stored in the registers from corruption. VORAGO Technologies architecture for implementing TMR in registers uses both a Dual Interlocked Storage Cell (DICE) and an EDAC and scrub approach.

Nodes within a DICE latch are cross-coupled. A latch cannot change state unless at least two of the three nodes within the latch are attempting to change state simultaneously. Under normal operation, system initiated changes to the state of a DICE latch will force all three nodes to change state, but in the event of a particle strike or other transient upset on only one of the three nodes, the state change is ignored and the switching node is forced back to matching the other two nodes comprising the latch. As an additional protection scheme, the position of the three nodes in each DICE latches are spatially separated and non-linear to reduce the likelihood of a single particle strike corrupting more than one node.

To further protect the registers from data corruption, Registers are protected using an EDAC scheme (where sufficient parity information is stored in register parity bits) to allow detection and correction of single bit errors within registers. These EDAC protected registers are periodically scrubbed to locate and correct bit upsets before they can accumulate.

As a third protection, some critical registers employ delay filtered DICE latches that ensures that transients below a specified minimum duration to the inputs of the register bits do not trigger a state change.

## VI. Power consumption

One of the challenges that has long faced designers of electronic systems that are subject to high temperatures is the tendency exhibited in CMOS circuits to consume a significantly higher amount of power as temperature increases. The processing adjustments that HARDSLIL® introduces and the transistor engineering that is unique to the VA10800 addresses this effect and significantly reduces the elevated core current consumption at elevated temperatures. Figure 5 illustrates a plot of operating frequency against temperature and exhibits an almost linear relationship across the temperature range. This is most unusual. Note that the maximum operating speed of the VA10800 is specified at 50MHz, although it is tested well beyond this range.

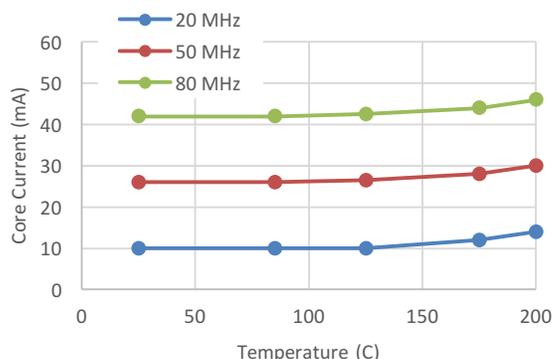


Figure 5 – VA10800 current consumption versus temperature characteristics

## V. Conclusion

This paper discussed the motivation behind creating ARM® Cortex®-M based microcontroller products for use in extreme environments and the innovations that underpin their ability to operate under conditions of high temperature and high radiation. Engineers want access to the latest technology that is the best fit for embedded systems – the provision of an ARM® Cortex®-M microcontroller that is designed for use in extreme environments satisfies this demand.

The mechanisms that lead to CMOS circuit failure have been addressed by a ground-up approach to immunize against latch-up, which is a more robust methodology than rooting out failing parts using testing and screening.

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